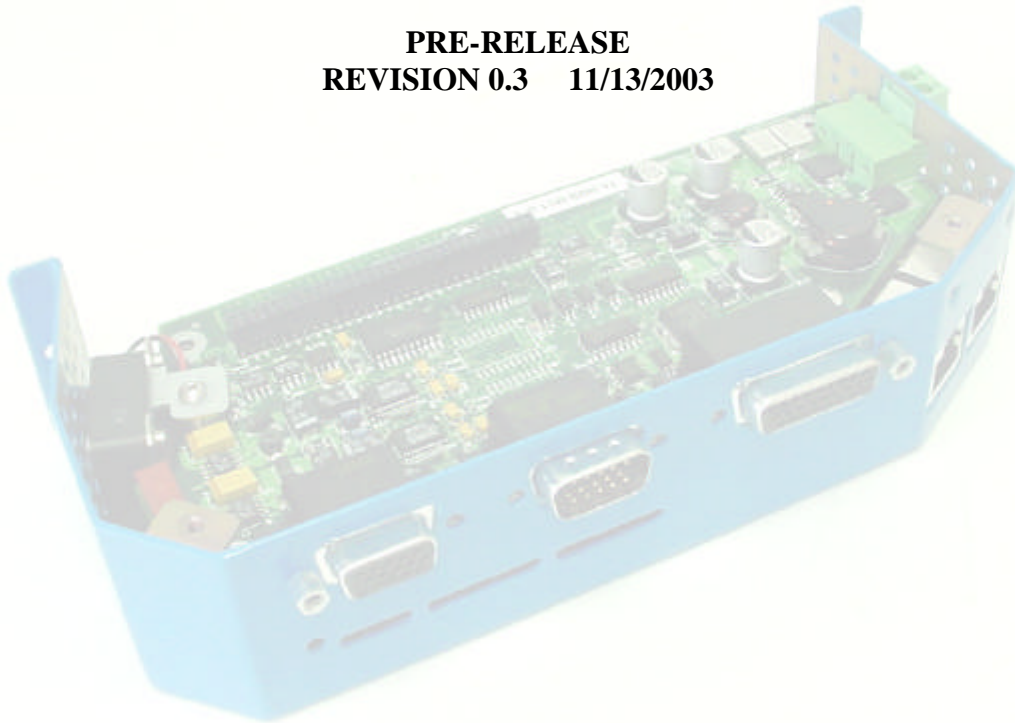


# SYNQNET™ REMOTE I/O BLOCK TA806 DIGITAL

PRE-RELEASE  
REVISION 0.3 11/13/2003



**Trust Automation Inc.**  
205 Suburban Road  
San Luis Obispo, CA 93401  
Phone (805) 544-0761  
Fax (805) 544-4621

**[WWW.TRUSTAUTOMATION.COM](http://WWW.TRUSTAUTOMATION.COM)**



## REVISION LIST

Date	Revision	Description	Author
7/18/2003	Rev 0	Initial Draft of Specification	Pat Scrivner
7/29/2003	Rev 0	Pre-release edits	Pat Scrivner
7/30/2003	Rev 0	Manual to Ty, Eric for review	Pat Scrivner
8/21/2003	Rev 0	1 <sup>st</sup> Round edits incorporated – beta release	Pat Scrivner
09/16/2003	Rev 0.1	Text only change in Section 3 – beta update	Pat Scrivner
10/08/2003	Rev 0.2	Updated Figure 6 – beta update	Pat Scrivner
11/13/2003	Rev 0.3	Incorporated RMB changes - major	Pat Scrivner



## TABLE OF CONTENTS

<b>1 SCOPE</b> .....	<b>5</b>
<b>2 DEFINITIONS</b> .....	<b>6</b>
<b>3 DESCRIPTION</b> .....	<b>7</b>
<b>4 FUNCTIONAL BLOCKS</b> .....	<b>11</b>
4.1 SYNQNET NETWORK INTERFACE	12
4.2 SYNQNET FPGA CORE	12
4.3 DIGITAL INPUT BLOCKS	13
4.4 DIGITAL OUTPUT BLOCKS	14
4.5 LED STATUS INDICATORS	15
4.5 AMPLIFIER FAULT INPUT	18
4.6 SHUTDOWN INPUT CIRCUIT	20
4.7 RIOB POWER INLET CIRCUIT	21
<b>5 CONNECTORS</b> .....	<b>22</b>
5.1 SYNQNET INTERFACE IN CONNECTOR (J1)	23
5.2 SYNQNET INTERFACE OUT CONNECTOR (J2)	24
5.3 POWER INLET CONNECTOR (J3)	25
5.4 DIGITAL OUTPUT CONNECTOR (J4)	26
5.5 DIGITAL INPUT CONNECTOR (J5)	28
<b>6 SPECIFICATIONS</b> .....	<b>30</b>
6.1 MECHANICAL DIMENSIONS	30
6.2 ELECTRICAL	31
6.3 ENVIRONMENTAL	32
6.4 COOLING REQUIREMENTS	33
<b>7 SOFTWARE</b> .....	<b>34</b>
7.1 REQUIRED SOFTWARE LEVELS	34
7.2 NODE_ALARM GENERATION	34
<b>APPENDIX A – PRODUCT OPTIONS</b> .....	<b>36</b>
<b>APPENDIX B – HARDWARE ERRATA</b> .....	<b>37</b>
<b>APPENDIX C – CONTACT INFORMATION</b> .....	<b>38</b>



## TABLE OF FIGURES

Figure 1 – SynqNet Network Block Diagram	8
Figure 2 – TA806 RIOB Functional Block Diagram	10
Figure 3 – Input Circuit	13
Figure 4 – Output Circuit	14
Figure 5 – Panel View of LED Status Indicators	17
Figure x – MT Fault Generation	18
Figure 6 – Shutdown Input Circuit	20
Figure 7 – Power Inlet Circuit	21
Figure 8 – J1 IN Connector Front View	23
Figure 9 – J2 OUT Connector Front View	24
Figure 10 – J3 Mating Connector Front View	25
Figure 11 – J4 Connector Front View	26
Figure 12 – J5 Connector Front View	28
Figure 13 – Mechanical Dimensions	30
Figure 14 – Mounting View	33



## 1 SCOPE

This manual documents the function and usage of the Trust Automation TA806 SynqNet™ Remote I/O Block (RIOB) series of Digital I/O products. These products are used in SynqNet-based networked motion control systems to provide digital input and output bit functions at SynqNet update rates. It is the goal of this manual to provide the user with information sufficient to support setup and normal use.

This manual pertains to the following TA806 products:

- TA806-D01 Digital RIOB, 16 input, 16 output, High Density DB connectors
- TA806-E01 Digital RIOB, 16 input only, High Density DB connector
- TA806-F01 Digital RIOB, 16 output only, High Density DB connector
  
- TA806-D21 Digital RIOB, 16 input, 16 output, High Density DB connectors, with Fan
- TA806-E21 Digital RIOB, 16 input only, High Density DB connector, with Fan
- TA806-F21 Digital RIOB, 16 output only, High Density DB connector, with Fan



## 2 DEFINITIONS

Throughout this manual, various terms and acronyms are used in discussion of SynqNet and the TA806 product family. Definition of those most commonly used follows:

- AIO Analog I/O
- AMP Amplifier or drive for motor
- Axis Reference to all components relating to a single axis of motion
- CAT5 Category 5 cabling
- DIO Digital I/O
- Ethernet IEEE 802.3b Physical Ethernet Standard for 100BASE-TX
- Flash Non-volatile memory or memory device
- FPGA Field Programmable Gate Array
- I/O Input/Output, generally refers to bitwise control
- LED Light Emitting Diode, used as status indicators
- Module SynqNet Node
- MT Module Over-Temperature condition
- Node Means 'slave-mode' and not the controller
- PHY Ethernet physical layer interface device
- PTC Positive Temperature Coefficient
- RING SynqNet network topology with return link
- RIOB Remote I/O Block, component of SynqNet network
- RMB Remote Motion Block, component of SynqNet network
- RT Relay Over-Temperature condition
- SSR Solid State Relay
- STRING SynqNet network topology without return link
- SynqNet™ A 100Mbit, full duplex motion control network devised by MEI

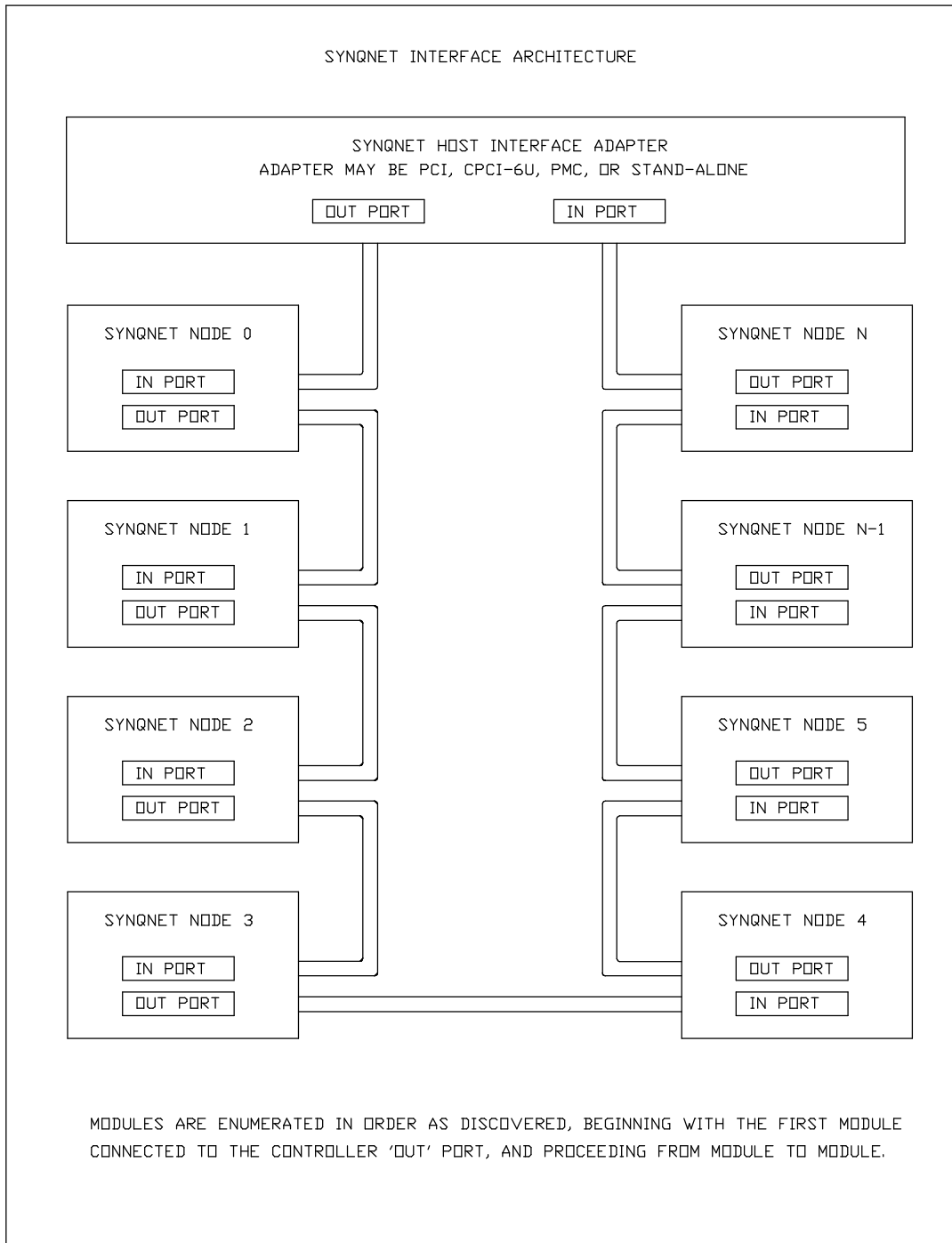


### 3 DESCRIPTION

The TA806 RIOB products communicate with a centralized, motion control network via the SynqNet™ standard interface developed by Motion Engineering Inc. SynqNet is an all-digital motion control interface for connections between motion controllers and drives. The physical layer of SynqNet is based on IEEE 802.3 standards for 100Base-X, the physical layer of Ethernet. The data link and application layers of SynqNet were designed by MEI. The 100Base-TX media system is based on specifications published in the ANSI TP-PMD physical media standard. The 100Base-TX system operates over two pairs of wires, one for receive data signals and one for transmit data signals. SynqNet is strictly master-slave in concept. There is no peer-to-peer communication. SynqNet is not compatible with Ethernet hubs or switches.

SynqNet networks can exist as one of two topologies, either 'RING' or 'STRING'. The ring topology provides the return link from the last node to the host controller, the string topology does not. Ring networks are fault-tolerant, and implement two full-duplex 100Mbit channels from the controller to the node(s). String networks are not fault-tolerant, and consist of one full-duplex 100Mbit channel from the controller to the node(s). The interface is made up of an Ethernet hardware layer, with redundant connections. Node link connections are electrically isolated at both ends. The inter-node cabling used is shielded CAT5 100BaseT or better. Shielding is recommended, but not required under the SynqNet specification. See Figure 1 for a representative example of a RING network with enumerated node ID's.





**FIGURE 1 – SYNQNET NETWORK BLOCK DIAGRAM**



The SynqNet cyclic rate can be approximated as shown in Table 1. The table lists expected network performance based solely on network loading.

# OF SINGLE-AXIS NODES	CYCLIC RATE
4	48KHz
8	24KHz
12	16KHz
20	10KHz
24	8KHz
48	4KHz

Table 1 – Cyclic Update Rate

Each TA806 RIOB module contains input and/or output circuitry specific to interface to general purpose sensors and controls. Each module occupies two axis of SynqNet network space, with each axis dedicated to the following functions:

- 24V 500mA digital outputs (8 per axis)
- 24V digital inputs (8 per axis)
- Capture input (1 per axis)

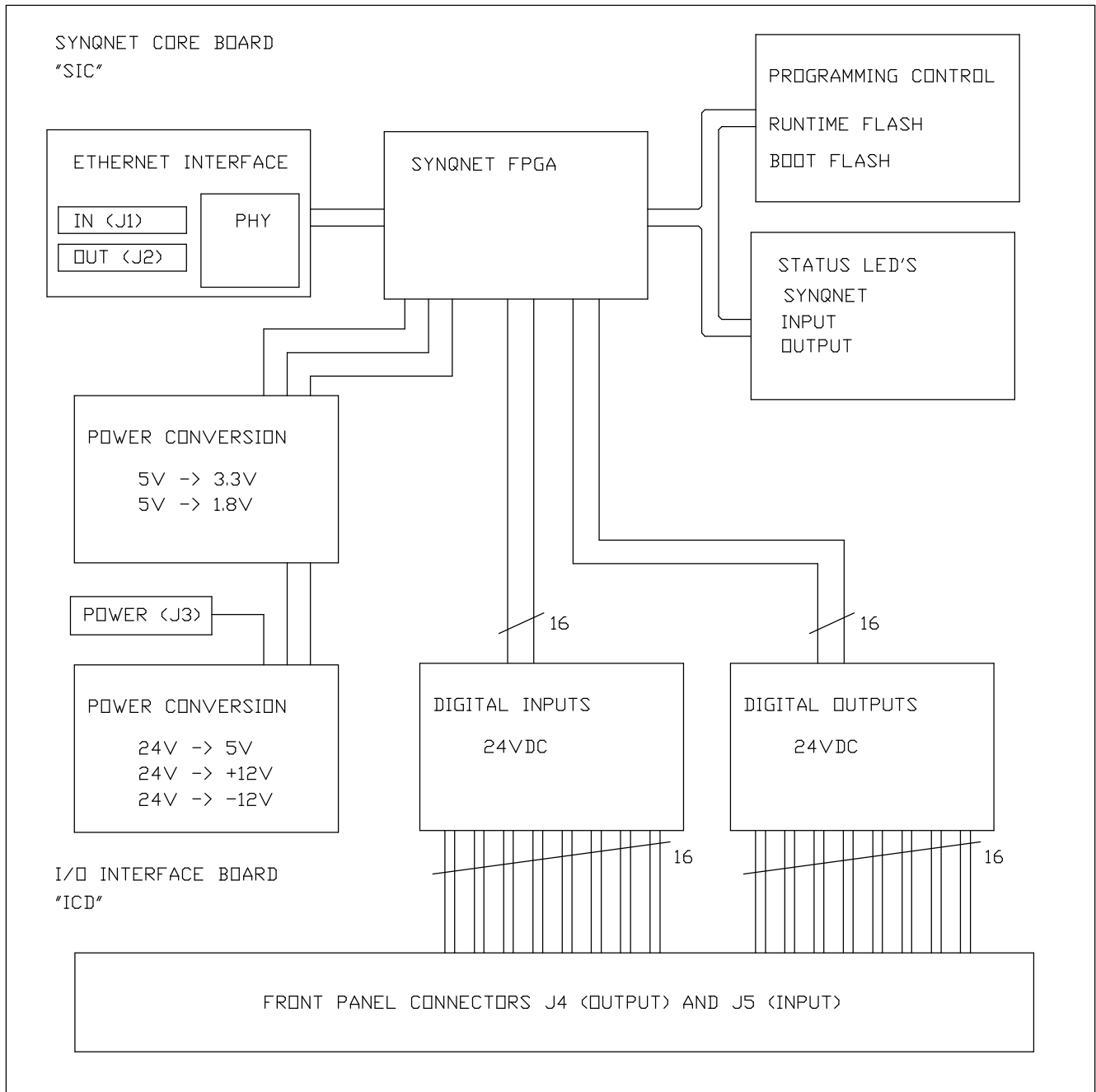
Digital inputs are optically isolated active-low circuits. All sixteen inputs are identical and are mapped as DI0 through DI7 (on axis 0) and as DI8 through DI15 (on axis 1). In addition, one of the eight inputs on each axis (IN0 on axis 0 and IN8 on axis 1) is associated with a high-speed capture engine. This provides two channels of high-speed capture per RIOB module.

Digital outputs are optically isolated active-high circuits. All sixteen outputs are identical and are mapped as DO0 through DO7 (on axis 0) and as DO8 through DO15 (on axis 1).

In addition, the TA806 modules contain a single shutdown input, configured as a differential, current-limited OPTO input.

The following block diagram shows the major functions of the TA806 RIOB.





**FIGURE 2 – TA806 RIOB FUNCTIONAL BLOCK DIAGRAM**



## 4 FUNCTIONAL BLOCKS

This section gives greater detail on each of the functional blocks of the RIOB. They are:

- SynqNet Ethernet Interface
- SynqNet FPGA Core
- Digital Input Blocks
- Digital Output Blocks
- LED Status Indicators
- AMP FAULT Circuit
- SHUTDOWN Circuit
- Power Inlet Circuit

Each of these blocks is outlined in the following sections.



## 4.1 SYNQNET NETWORK INTERFACE

The RIOB Ethernet interface adheres to IEEE 802.3 Physical Ethernet Standard for 100BASE-TX. The conformance is physical layer only; all higher levels are SynqNet proprietary. The Ethernet interface is composed of the following major components:

- Molex 85504 shielding modular (RJ-45) connectors, one for IN link and one for OUT link.
- Pulse H1102 10/100BASE-T Magnetics
- Broadcom BCM5222 10/100BASE-TX Dual-Port Transceiver
- Discrete filter components

The Broadcom physical layer interface (PHY) is programmed by the SynqNet FPGA, no direct user programming of the PHY is accessible.

The SynqNet network specification provides for use of RJ-45 style modular Ethernet connectors or Micro-D Subminiature (MDSM) connectors. The Trust Automation SynqNet product families use only modular connectors to provide a low-cost solution. The RIOB product family provides a cable support solution for use with RJ-45 cables. For additional details see Appendix A.

## 4.2 SYNQNET FPGA CORE

The SynqNet FPGA core controls all local execution of the RIOB module, directed by the SynqNet host interface controller. The core controls local in-situ programming of the RUNTIME Flash image, under network control.

Configuration data for the FPGA is stored as two unique images. The BOOT image is stored in one flash device. This device is programmed at the factory, and cannot be written or modified in the field.

The RUNTIME image is stored in a second flash device, is programmed at the factory, but can also be updated in the field by the user via the SynqNet interface. This gives the user the ability to update node firmware on all SynqNet nodes in his target system. After reset, the FPGA configuration data is normally loaded from the RUNTIME flash. If, during boot, the RUNTIME image is detected as corrupt or missing, the BOOT image is then loaded to allow the user to reprogram the RUNTIME image via the SynqNet network.

Node-specific hardware information is stored in an EEPROM located in the SynqNet core. Of interest to the user would be the Node type, serial number, and unique ID. This information allows the user to identify, via the SynqNet network, all node types present, and to identify any changes made to the network.



### 4.3 DIGITAL INPUT BLOCKS

The digital input circuits on the RIOB are designed to create a fault-tolerant 24V input interface. Each input block presents one input pin to the user, along with isolated 24Vdc and isolated return pins. The circuit block shown in Figure 3 is representative of all digital I/O inputs. Each input pin on the front panel connector is routed to the right side of the schematic, nets DI\_0 through DI\_3 are shown as examples. If the input pin is left unconnected or is connected to 24Vdc, the OPTO input stage is biased, and the FPGA sees a LOW, or inactive input. If the input pin is connected to 0Vdc, the OPTO stage is not biased, the FPGA sees a HIGH, or active input. The input circuits are active low, with a sink requirement of 8.0mA maximum. The user should implement external circuitry to connect a switch pole between the input pin and return pin, with the closed switch indicating an active input. Protection of the input photodiode with an external silicon diode is recommended if reverse voltages greater than 6Vdc will be present.

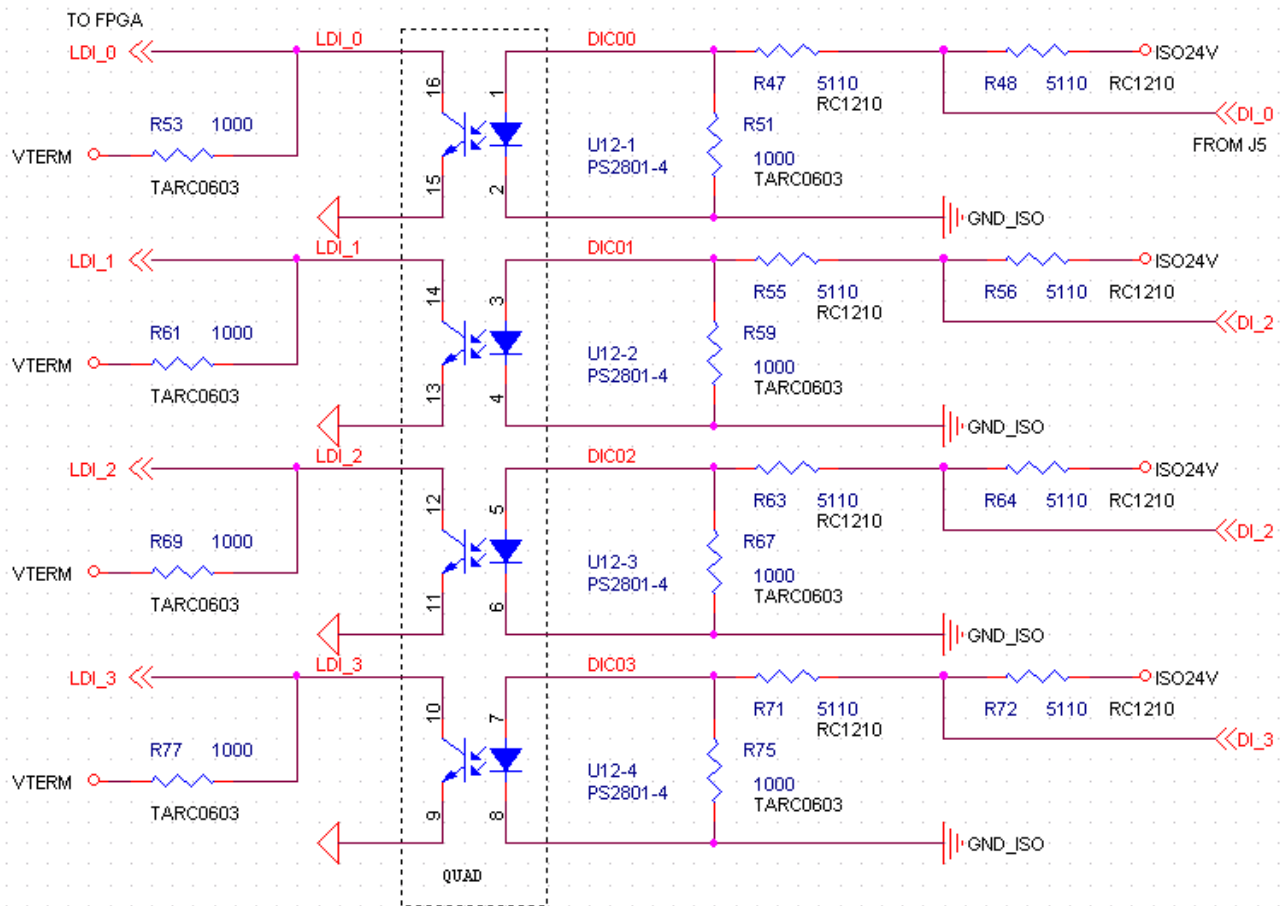


FIGURE 3 – INPUT CIRCUIT



### 4.4 DIGITAL OUTPUT BLOCKS

The digital output circuits on the RIOB are designed to create a fault-tolerant thermally-protected 24V output interface. Each output block presents one output pin to the user, along with an isolated return pin. The circuit block shown in Figure 4 is representative of all digital I/O outputs. OPTO-isolators are used to level-translate the FPGA outputs to 24Vdc. The translated outputs are then used to drive the input of high-current Solid State Relay (SSR) drivers. The relay driver output pins are connected directly to the front panel connector pins. The SSR contains over-temperature, over-current, under-voltage, and load demagnetization circuitry. No external protection is required.

If the output of the FPGA is asserted high, the OPTO stage is not biased, turning on the SSR driver output. If the output of the FPGA is asserted low, the OPTO stage is biased, turning off the SSR driver output. Note that although each SSR output is capable of 500mA, only 2.5A of total current is allowed for all 16 outputs.

The output circuits are described as active high. Any detected error is AND'd into the fault detection logic, which is then reported to the host as an amplifier fault. This operation is described in section 4.5.

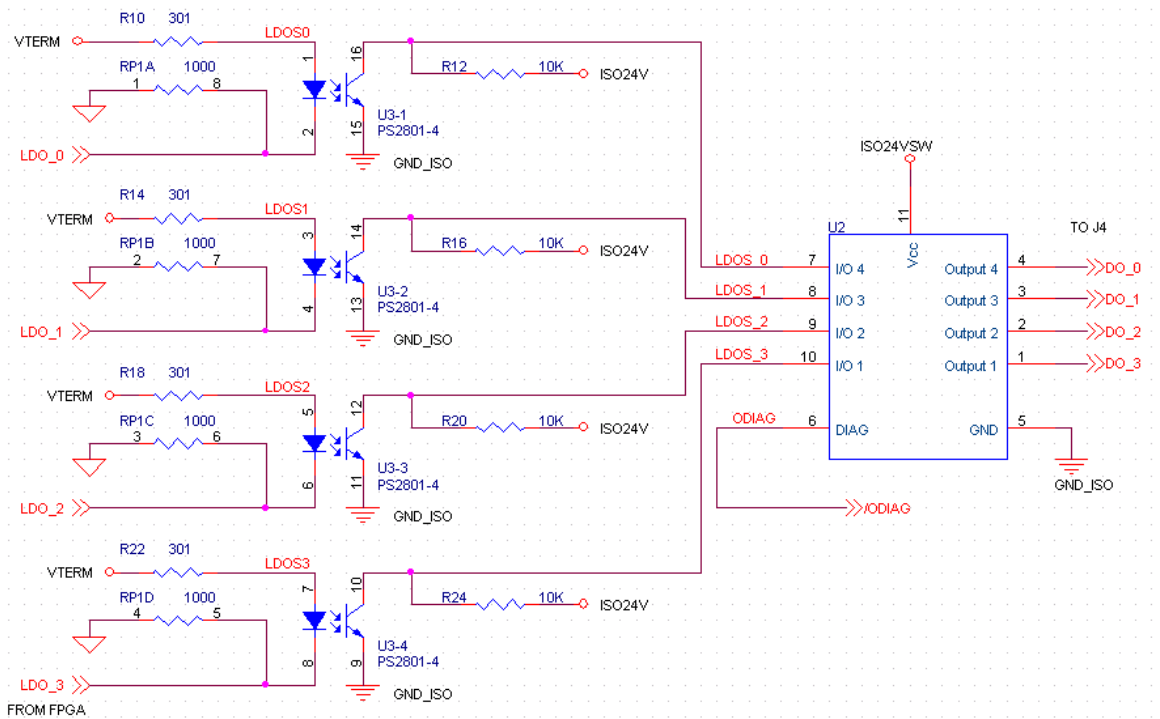


FIGURE 4 – OUTPUT CIRCUIT



## 4.5 LED STATUS INDICATORS

The RIOB module contains 39 status LED's which are all located on the front panel, next to J4 and J5. The status LED's for input and output are loaded only when those functions are present in the module. These LED's are assigned as follows:

- D1 though D6 are status LED's for the SynqNet interface
- D7 is a status LED indicating the FAULT status of OUT0 - OUT15
- D8 through D23 are status LED's for OUT0 – OUT15
- D24 through D39 are status LED's for IN0 – IN15

These indicators are displayed pictorially in the Figure 5 at the end of this section. The function of SynqNet status LED's D1 through D6 is as follows:

LED	Name	Color	Meaning when on	Controlled by	Modes
D1	<b>STATUS</b>	Blue	FPGA boot successful	FPGA	Off/Blink/On
D2	<b>NODE</b>	Green	Node state	FPGA	Off/Blink/On
D3	<b>REPEAT</b>	Green	Repeater ON	FPGA	Off/Blink/On
D4	<b>IN ACT</b>	Green	Link active	PHY	Off/On
D5	<b>OUT ACT</b>	Green	Link active	PHY	Off/On
D6	<b>ALARM</b>	Red	Node alarm exists	FPGA	Off/On

D1, D2, D3, and D6 are used to indicate normal node status as follows:

Node state	<b>STATUS</b> Blue (D1)	<b>NODE</b> Green (D2)	<b>REPEAT</b> Green (D3)	<b>ALARM</b> Red (D6)
Unpowered	OFF	OFF	OFF	OFF
Reset	OFF	OFF	OFF	OFF
Undiscovered	BLINK .37 Hz	BLINK (1)	OFF	ON
Discovered	BLINK .75 Hz	BLINK (1)	OFF	ON
SYNQ	ON	ON	ON or OFF (3)	OFF
SYNQ lost	BLINK 1.5 Hz	BLINK (2)	BLINK (4)	ON

- (1) Blinks in same phase as **STATUS**
- (2) Blinks in opposite phase of **STATUS**
- (3) On if not node N-1, otherwise off
- (4) Off if node 0, otherwise blink in same phase as **STATUS**

For **STRING** networks, if all nodes are in SYNC, the normal state of nodes 0 through node n-1 is to have **STATUS**, **NODE**, **REPEAT**, **IN ACT**, and **OUT ACT** continuously on. Node N (the last node) will have **STATUS**, **NODE**, and **IN ACT** continuously on.

For **RING** networks, if all nodes are in SYNC, the normal state of nodes 0 through node n-1 is to have **STATUS**, **NODE**, **REPEAT**, **IN ACT**, and **OUT ACT** continuously on. Node N (the last node) will



have **STATUS**, **NODE**, **IN ACT**, and **OUT ACT** continuously on.

LED D7 (RED) indicates that one of the D0-D15 output drivers has thermally faulted and shut down. See section 4.5 for additional details.

LED's D8 through D23 (GREEN) indicate the current state of OUT0 through OUT15, respectively. If the LED is on, the corresponding output has been asserted, providing a low-impedance path (0.4 ohm maximum) to the internal isolated 24Vdc supply (500 mA maximum, 1.5A total for all outputs). If the LED is off, the output has been de-asserted, providing a low voltage output (1.5V maximum at low current).

LED's D24 through D39 (GREEN) indicate the current state of IN0 through IN15, respectively. If the LED is on, the corresponding input is biased (24Vdc @ 5mA minimum). If the LED is off, the source of bias has been removed.



		RIOB	
STATUS	BLUE		D1
NODE	GREEN		D2
REPEAT	GREEN		D3
IN ACT	GREEN		D4
OUT ACT	GREEN		D5
ALARM	RED		D6
FAULT	RED		D7
AXIS 0 OUT 0	GREEN		D8
AXIS 0 OUT 1	GREEN		D9
AXIS 0 OUT 2	GREEN		D10
AXIS 0 OUT 3	GREEN		D11
AXIS 0 OUT 4	GREEN		D12
AXIS 0 OUT 5	GREEN		D13
AXIS 0 OUT 6	GREEN		D14
AXIS 0 OUT 7	GREEN		D15
AXIS 1 OUT 8	GREEN		D16
AXIS 1 OUT 9	GREEN		D17
AXIS 1 OUT 10	GREEN		D18
AXIS 1 OUT 11	GREEN		D19
AXIS 1 OUT 12	GREEN		D20
AXIS 1 OUT 13	GREEN		D21
AXIS 1 OUT 14	GREEN		D22
AXIS 1 OUT 15	GREEN		D23
AXIS 0 IN 0	GREEN		D24
AXIS 0 IN 1	GREEN		D25
AXIS 0 IN 2	GREEN		D26
AXIS 0 IN 3	GREEN		D27
AXIS 0 IN 4	GREEN		D28
AXIS 0 IN 5	GREEN		D29
AXIS 0 IN 6	GREEN		D30
AXIS 0 IN 7	GREEN		D31
AXIS 1 IN 8	GREEN		D32
AXIS 1 IN 9	GREEN		D33
AXIS 1 IN 10	GREEN		D34
AXIS 1 IN 11	GREEN		D35
AXIS 1 IN 12	GREEN		D36
AXIS 1 IN 13	GREEN		D37
AXIS 1 IN 14	GREEN		D38
AXIS 1 IN 15	GREEN		D39

**FIGURE 5 – PANEL VIEW OF LED STATUS INDICATORS**



### 4.5 AMPLIFIER FAULT INPUT

The RIOB can be programmed to generate a fault based on multiple types of input events. A fault usually generates a NODE\_ALARM condition. One of these input events is an amplifier fault from axis 0.

For axis 0 of the TA806 RIOB, the AMP FAULT input to the FPGA can be set active by either a Module over Temperature or an OUTPUT driver over Temperature (RT) condition.

For axis 1 of the TA806 RIOB, the AMP FAULT input to the FPGA cannot be set active by external events.

A solid-state temperature sensor is used to detect the internal temperature of the module. The sensor is located in the airflow path common to the FPGA. This sensor will be activated when the internal temperature of the module exceeds 72°F (22.2°C). This temperature sensor can be defeated from the amplifier chain as a manufacturing option. Contact Trust Automation for additional details.

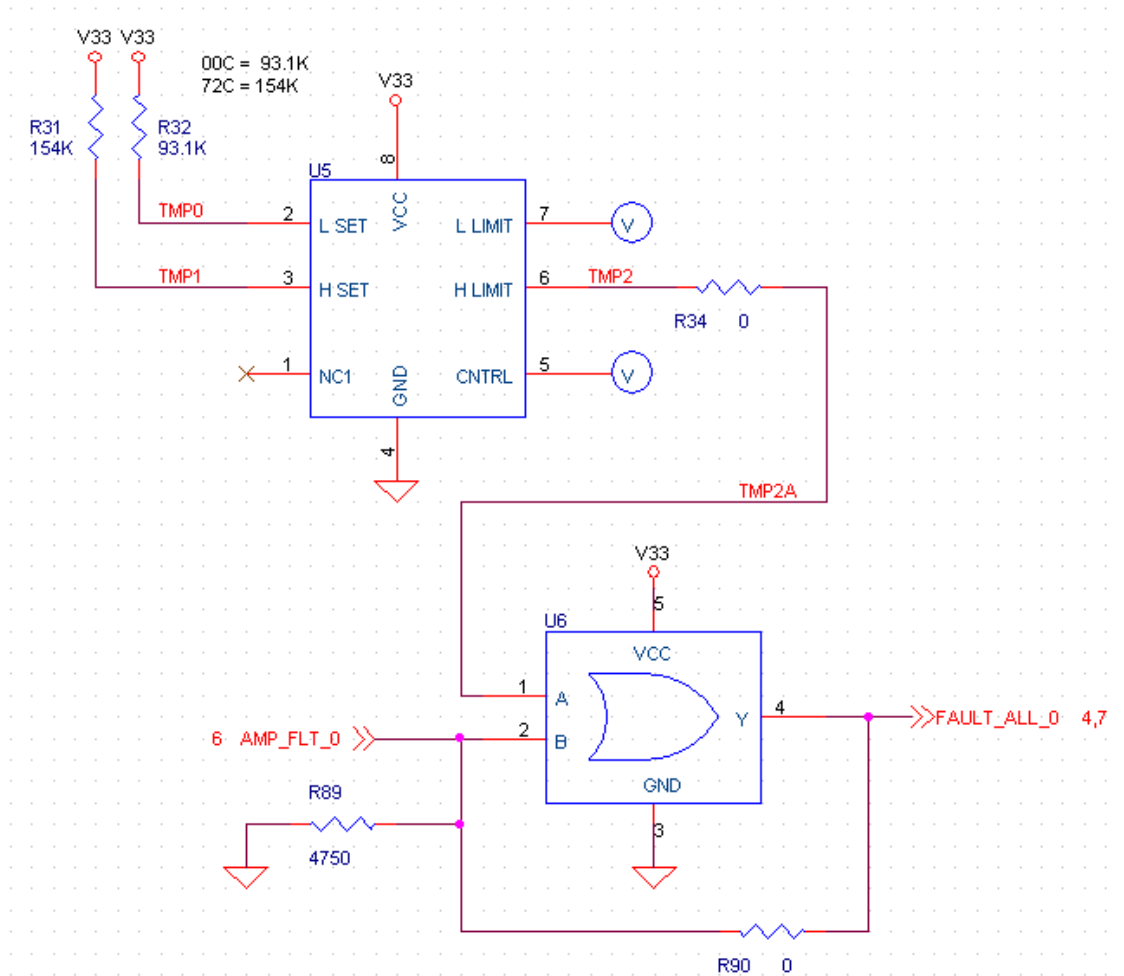


FIGURE 6 – MT FAULT GENERATION



Four solid state relay (SSR) drivers are used to provide 16 digital high-current outputs on the TA806 RIOB. Each of these SSR packages provides an output to indicate an over temperature condition within the device. The outputs of all 4 devices are OR'd together, and then AND'd into the axis 0 AMP FAULT chain. (*Errata: note that the RT outputs of all four devices generate a fault on axis 0, even though the outputs are distributed between axis 0 and axis 1.*)

The FPGA does not differentiate between MT and RT conditions. The most common scenario for the user upon detecting a NODE\_ALARM condition at the module is:

- If LED indicator D7 on the module frontplate is on, a RT condition exists. Disconnect all external cables from J4. Allow the SSR output drivers to cool for 2-3 minutes. D7 should turn off. If so, the source of the problem is generally wiring external to the RIOB module. Wiring and connectors should be examined and the fault corrected.
- If no amplifier fault exists and LED D7 is off, the module internal Over-Temperature has been triggered. The module operating conditions should be inspected to determine the nature of the fault.



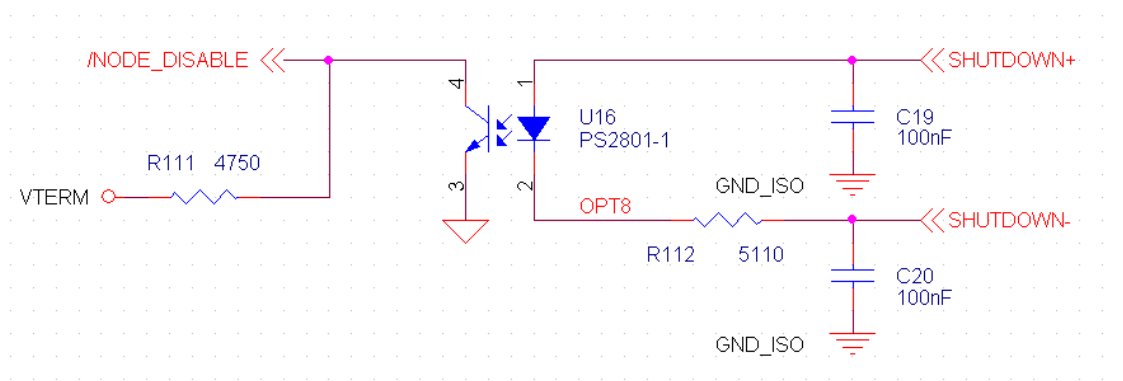
## 4.6 SHUTDOWN INPUT CIRCUIT

The RIOB implements a method for the user to initiate a node disable from an external source. This is done using the SHUTDOWN+ and SHUTDOWN- pins on the OUTPUT connector J4. Assertion (bias) of the SHUTDOWN input will disable the node.

The SHUTDOWN+ pin (pin 40) and the SHUTDOWN- pin (pin 41) are connected to the anode and cathode legs (respectively) of an OPTO-isolator, limited internally with a 5.11K resistor. The user can elect to bias the OPTO input circuit as a high-side switch or a low-side switch. Bias must be applied externally, using J4 pin 39 (ISO24V), one of the isolated ground return pins, and the user switch or control.

- If the input is disconnected or not biased, SHUTDOWN is not asserted. Note that this is the default state with no user connection.
- If the input is biased on, SHUTDOWN is asserted. This means disable the node.

The RIOB contains only one SHUTDOWN input circuit for use with both axes. See Figure 7 for circuit details.

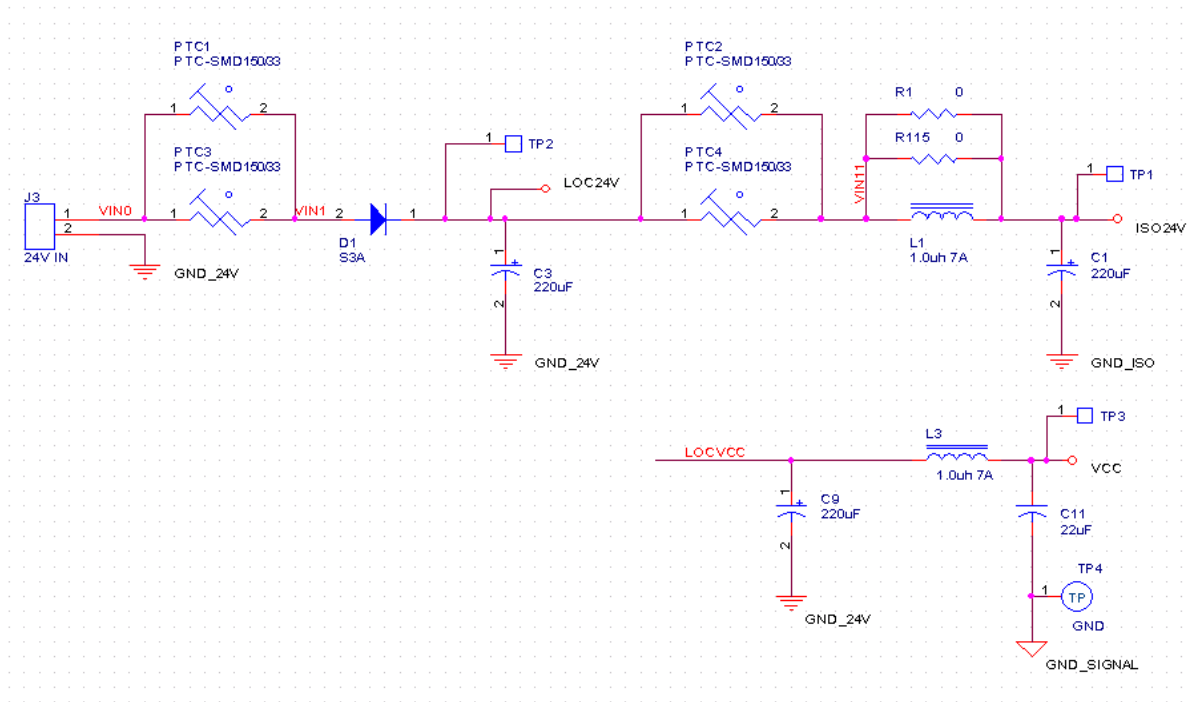


**FIGURE 7 – SHUTDOWN INPUT CIRCUIT**



### 4.7 RIOB POWER INLET CIRCUIT

Figure 8 shows the circuit protection elements in the power inlet stage. This circuit block is provided for reference only. Note that a 3A PTC combination and blocking diode protect the J3 24V input path. The isolated 24V supply present on the frontplate connectors is protected by a 2.5A PTC.



**FIGURE 8 – POWER INLET CIRCUIT**



## 5 CONNECTORS

The RIOB contains several panel connectors for external connections. These are designated as follows:

- J1 – SynqNet Interface IN connector
- J2 – SynqNet Interface OUT connector
- J3 – 24VDC power inlet connector
- J4 – Digital OUT connector
- J5 – Digital IN connector

Each connector type and style is described in additional detail in the following sections.



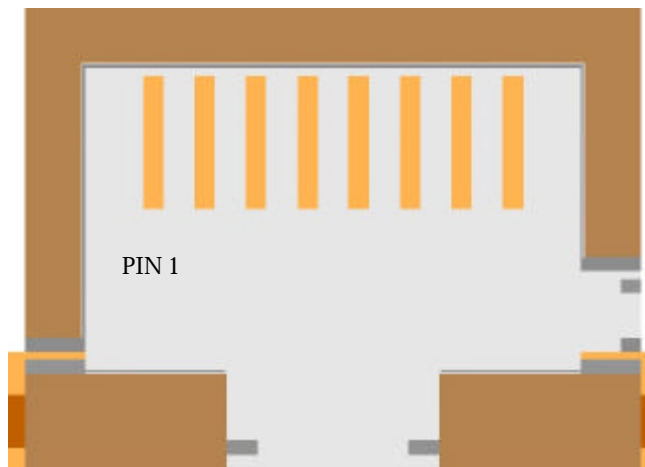
## 5.1 SYNQNET INTERFACE IN CONNECTOR (J1)

The SynqNet IN J1 connector is located on the bottom angled edge of the RIOB module. The connector is an RJ-45 style connector, is labeled as 'IN', and is the RJ-45 connector closest to the front (DB connectors) of the module. The board mounted connector is a Molex 85504-0001. Note that the Molex 85504 connector provides connectivity for shielded Ethernet cables. Shielded cables are recommended for the SynqNet interface but are not required. A representative mating shielded connector could be Molex 95043 Family or equivalent.

PIN	SIGNAL
1	TXD+
2	TXD-
3	RXD+
4	CT
5	CT
6	RXD-
7	CT
8	CT
SHIELD	*

\* The cable shield is capacitively coupled to the chassis, or frame.

Table 2 – SynqNet IN Port Pin Functions



**FIGURE 9 – J1 IN CONNECTOR FRONT VIEW**



## 5.2 SYNQNET INTERFACE OUT CONNECTOR (J2)

The SynqNet OUT J2 connector is also located on the bottom angled edge of the RIOB module. The connector is an RJ-45 style connector, is labeled as 'OUT', and is the RJ-45 connector closest to the rear (bulkhead flange) of the module. The board mounted connector is a Molex 85504-0001. Note that the Molex 85504 connector provides connectivity for shielded Ethernet cables. Shielded cables are recommended for the SynqNet interface but are not required. A representative mating shielded connector could be Molex 95043 Family or equivalent.

PIN	SIGNAL
1	RXD+
2	RXD-
3	TXD+
4	CT
5	CT
6	TXD-
7	CT
8	CT
SHIELD	*

\* The cable shield is capacitively coupled to the chassis, or frame.

Table 3 – SynqNet OUT Port Pin Functions

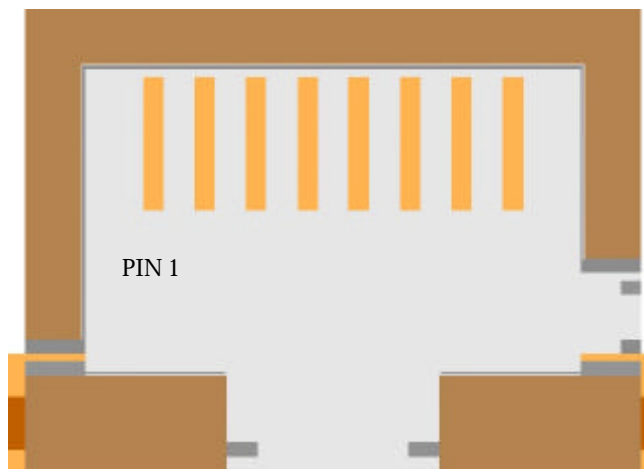


FIGURE 10 – J2 OUT CONNECTOR FRONT VIEW

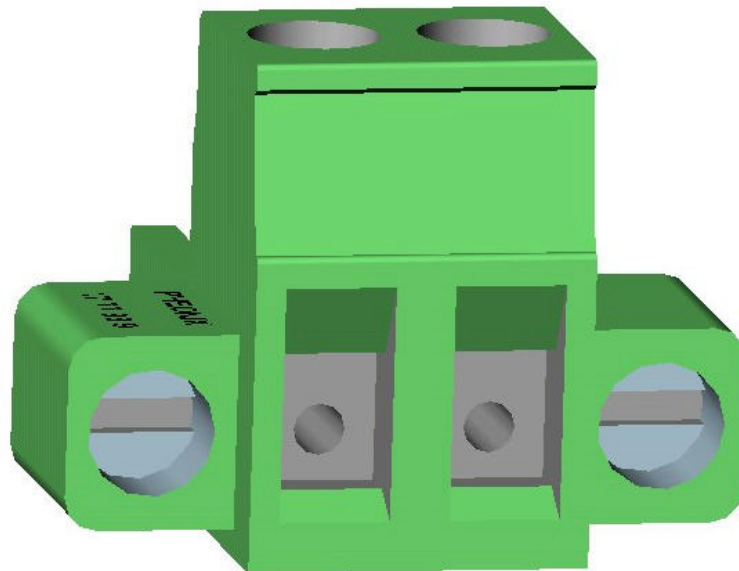


### 5.3 POWER INLET CONNECTOR (J3)

The power inlet connector J3 is located on the bottom of the RIOB SynqNet module. The board mounted connector is a Phoenix Contact Combicon™ family P/N 17 76 50 8. The external mating connector is a Phoenix Contact P/N 17 77 98 9 (TPN CON-0455-M1), and is supplied with every RIOB module. Note that the Phoenix Contact connector accepts wires sizes between 12 and 24 AWG. The required RIOB inlet voltage is 24VDC +/- 3VDC. The RIOB inlet power path is protected with a 3A PTC and a 3A blocking diode.

The RIOB provides isolated 24Vdc to the user via front panel connectors J4 (pin 39) and J5 (pins 31-42). Note this 24V source is isolated from the inlet supply with a 1.5A resettable circuit protection device (PTC).

Note: If the RIOB input voltage is 24.0Vdc, the isolated 24VDC provided to the user on front panel connectors J4 and J5 will be between 23.2 and 23.4 Vdc. This is due to the voltage drop of the protection device and blocking diode.



Source  
Positive

Return  
Negative

**FIGURE 11 – J3 MATING CONNECTOR FRONT VIEW**



### 5.4 DIGITAL OUTPUT CONNECTOR (J4)

The J4 connector is a 44 pin female high density D-Sub connector. The connector used in the RIOB is a Kycon K66-B44S-N. A representative mating connector is NORCOMP 180-044-102-001 (solder cup) or NORCOMP 180-044-172-000 (crimp and poke). A representative backshell kit is NORCOMP 977-025-020-121.

The following Figure and Tables detail the pin assignments and definitions of J4:

RIOB - J4					
DIGITAL OUT					
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	DO0	16	IRTN	31	NC
2	DO2	17	IRTN	32	NC
3	DO3	18	IRTN	33	NC
4	DO4	19	IRTN	34	NC
5	DO5	20	IRTN	35	NC
6	DO6	21	IRTN	36	NC
7	DO7	22	IRTN	37	NC
8	DO8	23	IRTN	38	FRAME
9	DO9	24	IRTN	39	ISO24V
10	DO10	25	IRTN	40	SHUTDOWN+
11	DO11	26	IRTN	41	SHUTDOWN-
12	DO12	27	IRTN	42	IRTN
13	DO13	28	IRTN	43	IRTN
14	DO14	29	IRTN	44	IRTN
15	DO15	30	DO16		

Table 4 – J4 Pin Assignments

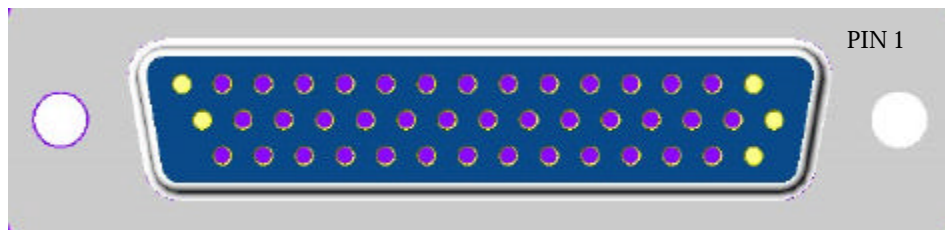


FIGURE 12 – J4 CONNECTOR FRONT VIEW



PIN	Definition	PIN	Definition
1	Digital Output 0	27	Isolated GND Return
2	Digital Output 1	28	Isolated GND Return
3	Digital Output 2	29	Isolated GND Return
4	Digital Output 3	30	Digital Output 15
5	Digital Output 4	31	Not Connected
6	Digital Output 5	32	Not Connected
7	Digital Output 6	33	Not Connected
8	Digital Output 7	34	Not Connected
9	Digital Output 8	35	Not Connected
10	Digital Output 9	36	Not Connected
11	Digital Output 10	37	Not Connected
12	Digital Output 11	38	FRAME/Chassis Connection
13	Digital Output 12	39	Isolated 24V
14	Digital Output 13	40	Shutdown+ Input
15	Digital Output 14	41	Shutdown- Input
16	Isolated GND Return	42	Isolated GND Return
17	Isolated GND Return	43	Isolated GND Return
18	Isolated GND Return	44	Isolated GND Return
19	Isolated GND Return		
20	Isolated GND Return		
21	Isolated GND Return		
22	Isolated GND Return		
23	Isolated GND Return		
24	Isolated GND Return		
25	Isolated GND Return		
26	Isolated GND Return		

Table 5 – J4 Pin Definitions



### 5.5 DIGITAL INPUT CONNECTOR (J5)

The J5 connector is a 44 pin male high density D-Sub connectors. The connector used in the RIOB is a Kycon K66-B44P-N. A representative mating connector is NORCOMP 180-044-202-001 (solder cup) or NORCOMP 180-044-272-000 (crimp and poke). A representative backshell kit is NORCOMP 977-025-020-121.

The following Figure and Tables detail the pin assignments and definitions of J5:

RIOB - J5					
DIGITAL IN					
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	DI0	16	IRTN	31	ISO24V
2	DI1	17	IRTN	32	ISO24V
3	DI2	18	IRTN	33	ISO24V
4	DI3	19	IRTN	34	ISO24V
5	DI4	20	IRTN	35	ISO24V
6	DI5	21	IRTN	36	ISO24V
7	DI6	22	IRTN	37	ISO24V
8	DI7	23	IRTN	38	ISO24V
9	DI8	24	IRTN	39	ISO24V
10	DI9	25	IRTN	40	ISO24V
11	DI10	26	IRTN	41	ISO24V
12	DI11	27	IRTN	42	IRTN
13	DI12	28	IRTN	43	DI15
14	DI13	29	IRTN	44	FRAME
15	DI14	30	IRTN		

Table 6 – J5 Pin Assignments

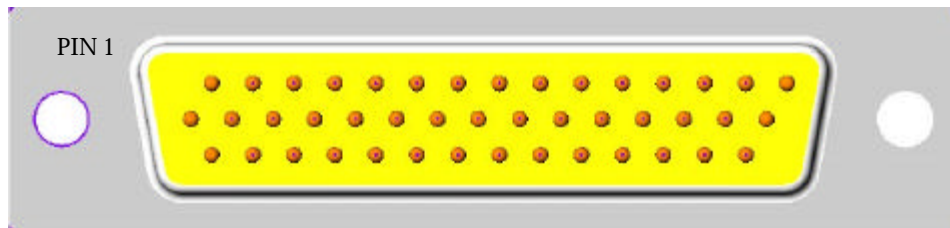


FIGURE 13 – J5 CONNECTOR FRONT VIEW



PIN	Definition	PIN	Definition
1	Digital Input 0	27	Isolated GND Return
2	Digital Input 1	28	Isolated GND Return
3	Digital Input 2	29	Isolated GND Return
4	Digital Input 3	30	Isolated GND Return
5	Digital Input 4	31	Isolated 24V
6	Digital Input 5	32	Isolated 24V
7	Digital Input 6	33	Isolated 24V
8	Digital Input 7	34	Isolated 24V
9	Digital Input 8	35	Isolated 24V
10	Digital Input 9	36	Isolated 24V
11	Digital Input 10	37	Isolated 24V
12	Digital Input 11	38	Isolated 24V
13	Digital Input 12	39	Isolated 24V
14	Digital Input 13	40	Isolated 24V
15	Digital Input 14	41	Isolated 24V
16	Isolated GND Return	42	Isolated GND Return
17	Isolated GND Return	43	Digital Input 15
18	Isolated GND Return	44	FRAME/Chassis Connection
19	Isolated GND Return		
20	Isolated GND Return		
21	Isolated GND Return		
22	Isolated GND Return		
23	Isolated GND Return		
24	Isolated GND Return		
25	Isolated GND Return		
26	Isolated GND Return		

Table 7 – J5 Pin Definitions

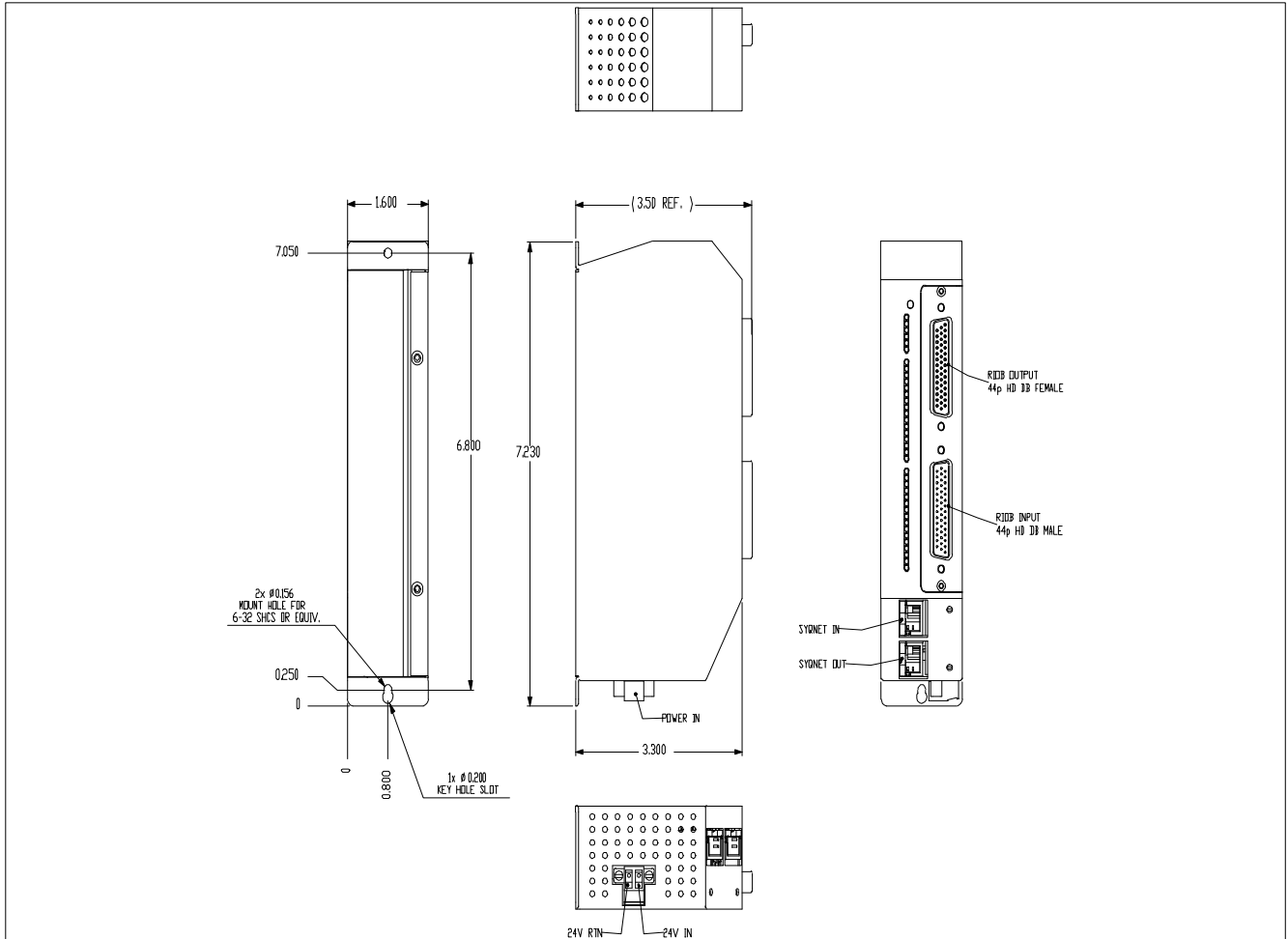


## 6 SPECIFICATIONS

This section lists the mechanical, electrical, and environmental specifications for the TA806 RIOB module family.

### 6.1 MECHANICAL DIMENSIONS

This section details the basic mechanical dimensions of the TA806 RIOB modules. Overall size and mounting locations are provided.



**FIGURE 14 – MECHANICAL DIMENSIONS**



## 6.2 ELECTRICAL

### INPUT POWER REQUIREMENTS

The RIOB requires the following input power based on internal and external usage. Internal usage is consumed within the module by internal circuitry, external usage is dissipated external to the module via user components connected to the various power source and return pins on J4 and J5. Input voltage, current, and power requirements for the TA806 RIOB modules with no external usage are:

- Input Voltage: 24V +/- 3.0VDC, ripple/noise less than 300mVDC peak
- Input Current 290mA typical, 415mA maximum
- Input Power 10W (max)

### USER POWER CAPABILITIES

External power usage is not considered part of the thermal cooling requirements for the module, but the user must account for external power usage in the system power budget.

- External 24V 2.5A maximum, 60W maximum

The RIOB can provide 24VDC power for external devices via the J4 and J5 front panel connectors. Available on J4 pin 39, and also on J5 pins 31 through 42. These power pins are all connected in common and protected by a 2.5A circuit protection device (PTC).

### ETHERNET

Ethernet Input/Output IEEE 802.3 100Base-TX (physical layer only)  
 100Base-T CAT 5 or better cabling required  
 Shielded cables recommended but not required  
 100m length per link (max)

### SIGNAL REQUIREMENTS

Shutdown Input ON = 24Vdc @ 5 mA (min), OFF = no bias  
 Digital Inputs OFF = 24Vdc (or disconnect), ON= 1.0Vdc @ 10 mA minimum  
 Digital Outputs ON = 24.0Vdc @ 500mA (max. each), OFF = no bias  
**The total 24V current for all 16 outputs is limited to 2.5A dc.**



### 6.3 ENVIRONMENTAL

<b>OPERATING TEMPERATURE:</b>	0°C (min) to 50°C (max)
<b>TEMPERATURE CHANGE</b>	10°C per hour (max)
<b>HUMIDITY</b>	0% to 95% Relative Humidity, non-condensing
<b>VIBRATION</b>	1.5mm (0.060") P-P sinusoidal
<b>SHOCK</b>	30g half sine shock 11msec individual axis

Exceptions to the product vibration and shock are Ethernet connectors. The specifications for the Molex 85504-0001 modular jacks used on the production RIOB modules are as follows:

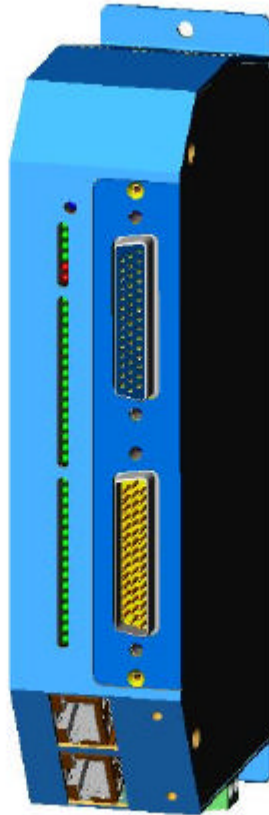
<b>MFGR Spec:</b>	Molex PS-85505 FCC Part 68, Subpart F
<b>Vibration:</b>	1.5mm (0.060") P-P 10-55-10 Hz sweep per minute 2 hours in each X-Y-Z axis
<b>Shock:</b>	No discontinuities greater than 1 usec 50g three sawtooth waveform shocks in each X-Y-Z axis No discontinuities greater than 1 usec
<b>Mating Family:</b>	95043 Series

Note that the RIOB product family provides for the use of cable support brackets with Ethernet cables plugged into connectors J1 and J2. See the Appendix A for additional details.



## 6.4 COOLING REQUIREMENTS

The TA806 RIOB can dissipate up to 10W internally. Convective cooling requires mounting the RIOB vertically, as shown below. 1.5 inches of clearance is required both above and below the module for convective cooling airflow.



**FIGURE 15 – MOUNTING VIEW**

For special mounting considerations or environments, internally mounted fan-forced cooling is available as a manufacturing option. For available product options see Appendix A. When the internal forced cooling is used the RIOB module may be mounted either horizontally or vertically. It should not be mounted in an inverted orientation (meaning with J3 on top).



## 7 SOFTWARE

This section discusses required software and firmware levels for the RIOB and host system. There is also a brief explanation of how node alarm is generated for the TA806 RIOB module family.

### 7.1 REQUIRED SOFTWARE LEVELS

The RIOB requires certain minimum revision levels of software and firmware in order to function correctly. These required minimum levels are:

MPI Firmware:	Version 510 Option 0
MPI DLL:	Version 20031023
MPI Version:	Version 20031023
MEI Host Firmware:	XMP510A1
FPGA Runtime Version:	0x020E0300

### 7.2 NODE\_ALARM GENERATION

The TA806 RIOB module has a status LED (D6) on the front panel that indicates alarm status. This LED is illuminated when a NODE\_ALARM state exists. The node can generate this alarm based on numerous inputs.

NODE\_ALARM is always active during power-on-reset, and during FPGA hardware configuration. This is due to external termination on the FPGA. NODE\_ALARM is also active while the FPGA BOOT image is being loaded from Flash. Once the FPGA is configured with the RUNTIME image, software can configure the FPGA NODE\_ALARM and I/O\_ABORT mask registers. The FPGA defaults to having NODE\_ALARM active when the network is not up. Software can override this during the discovery process. An active I/O\_ABORT state or a NODE\_ALARM state will create an alarm only if the mask registers have been configured to allow the fault to propagate.

The inputs to the mask register for the FPGA NODE\_ALARM signal are:

- I/O\_ABORT
- Node Not Cyclic
- AMP\_FAULT Axis 0
- AMP\_FAULT Axis 1

These fault sources can be individually masked or enabled by software. In the TA806 RIOB design, the AMP\_FAULT inputs from axis 0 consists of the following sources:

- RT Fault (thermal shutdown signal for all output drivers)
- MT Fault (thermal fault from module internal temperature sensor)

Note that the RT fault detected by axis 0 is actually the fault signal for all 16 output drivers, on both axis 0 and axis 1. Software cannot determine which axis originated the fault.

The inputs to the mask register for the I/O\_ABORT signal are:



- Sync Lost (the node has lost the SYNQ signal, and therefore is no longer under software control)
- Node disable (from SHUTDOWN input on J4)
- User (trigger from controller memory address)

These fault sources can be individually masked or enabled by software.

Note that an I/O Abort state will force all FPGA I/O pins to be inputs, thus tri-stating all outputs. Termination external to the FPGA will keep all I/O circuitry in required default states.



## APPENDIX A – PRODUCT OPTIONS

TA806 products can be ordered with several options. These options are detailed in the following section.

### Ethernet Cable Clamp Option

A cable clamping option may be attached to any TA806 RIOB module. When attached, this bracket clamps the Ethernet cables in place, minimizing movement of the Ethernet cables relative to the module. The cable clamping option is ordered as:

P/N: SUBZ-0803-A01

### Cooling Fan Option

Any TA806 RIOB module may be ordered with a cooling fan option. This 2.0 CFM fan, installed internally to the module during manufacturing, is recommended if horizontal mounting is expected. The fan option is ordered as shown in the following table:

Product Family	P/N without Fan	P/N with Fan
TA806	TA806-D01	TA806-D21
	TA806-E01	TA806-E21
	TA806-F01	TA806-F21

Table 8 – Fan Option Numbering



## APPENDIX B – HARDWARE ERRATA

Hardware changes occurred during the development of the TA806 RIOB. These changes are detailed below.

- Prototype RIOB modules (containing SIC PCB-0804-01 Rev 0) were shipped to customers and beta-sites with Ethernet connectors that would not guarantee isolation between the connector shields and the chassis. This was revised after the first round of prototypes.
- Prototype RIOB modules used AMP 406541-1 (or -5) for the Ethernet connectors. After the first prototype run the connectors were changed to Molex 85504-0001.
- Prototype RIOB modules (containing SIC PCB 0804-01 Rev 0) were shipped to early customers and beta-sites with 16 inputs mapped to axis 0 and 16 outputs mapped to axis 1. This allowed only one high-speed capture engine on input 0. Three units existed, all subsequent units were mapped as 8 in / 8 out per axis. Note that the RT fault generation from all 16 outputs has always been mapped to axis 0, for both 16/16 and 8/8 designs.
- Prototype RIOB modules (containing ICD PCB-0806-01 Rev 0) were shipped to early customer and beta-sites with input blocks configured with 0603 and 1206 resistors. These resistor package sizes were increased to 1210 on subsequent modules (containing ICD PCB-0806-01 Rev A).



## APPENDIX C – CONTACT INFORMATION

### Do you have hardware Questions?

Any hardware questions regarding use and operation of the Trust Automation TA801 and TA802 RMB family of products should be directed to:

Trust Automation, Incorporated  
205 Suburban Road  
San Luis Obispo, CA 93401

Corporate Office Telephone: (805) 544-0761  
Corporate Office Facsimile: (805) 544-4621

Corporate Website: [www.trustautomation.com](http://www.trustautomation.com)  
Email: [support@trustautomation.com](mailto:support@trustautomation.com)

### Do you have software Questions?

Any questions regarding use and operation of MEI XMP software with the TA801 and TA802 RMB family of Digital I/O products should be directed to:

Motion Engineering, Incorporated  
33 South La Patera Lane  
Santa Barbara, CA 93117-3214

Corporate Office Telephone: (805) 681-3300  
Corporate Office Facsimile: (805) 681-3311

Corporate Website: [www.motioneng.com](http://www.motioneng.com)  
Email: [info@motioneng.com](mailto:info@motioneng.com)

Additional information regarding the SynqNet Interface Standard can be found at:

[http://www.synqnet.org/tech\\_library.html](http://www.synqnet.org/tech_library.html)

Additional information regarding connectors and other components can be found at the following websites:

Molex Website: [http://www.molex.com/cgi-bin/bv/molex/index\\_login.jsp](http://www.molex.com/cgi-bin/bv/molex/index_login.jsp)

Phoenix Contact Website: <http://www.phoenixcon.com/>

Tyco/Raychem Website: <http://www.raychem.com/>

Kycon Website: <http://www.kycon.com>

NORCOMP Website: <http://www.norcomp.net/>



## Index

cable clamping option, 34  
Contact Information, 36  
Digital Signal Requirements, 30  
fan cooling option, 34  
Humidity, 31  
J1 connector, 22  
J2 connector, 23  
J3 connector, 24  
J4 connector, 25  
J5 connector, 27  
mounting considerations, 32  
network performance, 9  
node disable, 19  
Operating Temperature, 31  
Shock, 31  
Temperature change, 31  
User Power Capabilities, 30  
Vibration, 31  
wires sizes, 24

©2003, Trust Automation, Incorporated.  
All Rights Reserved

