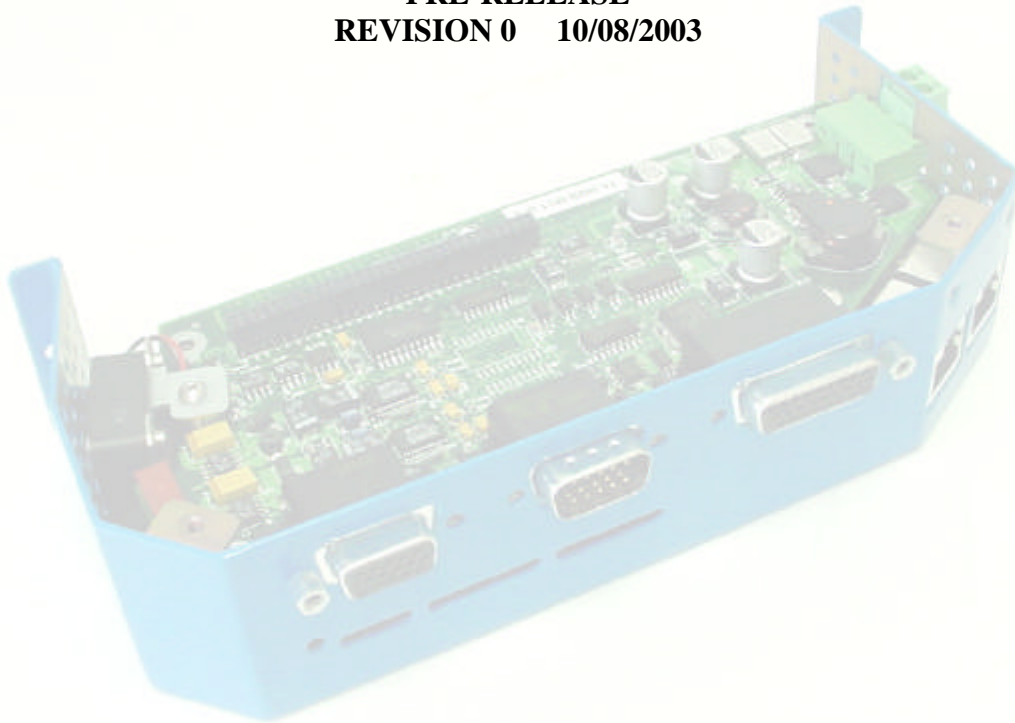


SYNQNET™ REMOTE I/O BLOCK TA805 ANALOG

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REVISION HISTORY

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1 SCOPE

This manual documents the function and usage of the Trust Automation TA805 SynqNet™ Remote I/O Block (RIOB) series of Analog I/O products. These products are used in SynqNet-based networked motion control systems to provide analog input and output functions at SynqNet update rates. It is the goal of this manual to provide the user with product information sufficient to support setup and normal use.

This manual pertains to the following TA805 products:

- TA805-D01 Analog RIOB, 8 input, 4 output, High Density DB connectors
- TA805-E01 Analog RIOB, 8 input only, High Density DB connector
- TA805-F01 Analog RIOB, 4 output only, High Density DB connector

2 DEFINITIONS

Throughout this manual, various terms and acronyms are used in discussion of SynqNet and the TA805 product family. Definition of those most commonly used follows:

- AIO Analog I/O
- Axis Reference to all components relating to a single axis of motion
- CAT5 Category 5 cabling
- Ethernet IEEE 802.3b Physical Ethernet Standard for 100BASE-TX
- Flash Non-volatile memory or memory device
- FPGA Field Programmable Gate Array, core device of RIOB
- I/O Input/Output, generally refers to bitwise control
- LED Light Emitting Diode, used as status indicators
- MT Module Over-Temperature condition
- Node Means 'slave-mode' and not the controller
- PHY Ethernet physical layer interface device
- RING SynqNet network topology with return link
- RIOB Remote I/O Block, component of SynqNet network
- RMB Remote Motion Block, component of SynqNet network
- STRING SynqNet network topology without return link
- SynqNet™ A 100Mbit, full duplex motion control network devised by MEI



3 DESCRIPTION

The RIOB products communicate with a centralized, motion control network via the SynqNet™ interface standard developed by Motion Engineering Inc. SynqNet is strictly master-slave in concept. There are no peer-to-peer communications. SynqNet is not compatible with Ethernet hubs or switches.

SynqNet networks can exist as one of two topologies, either 'RING' or 'STRING'. The ring topology provides the return link from the last node, the string topology does not. Ring networks are fault-tolerant, and implement two full-duplex 100Mbit channels from the nodes to the controller. String networks are not fault-tolerant, and consist of one full-duplex 100Mbit channel from the nodes to the controller. The interface is made up of an Ethernet hardware layer, with redundant connections. Node link connections are electrically isolated at both ends. The inter-node cabling used is shielded CAT5 100BaseT or better. (Shielding is recommended, but not required.) See Figure 1 for a representative example of a RING network with enumerated node ID's.

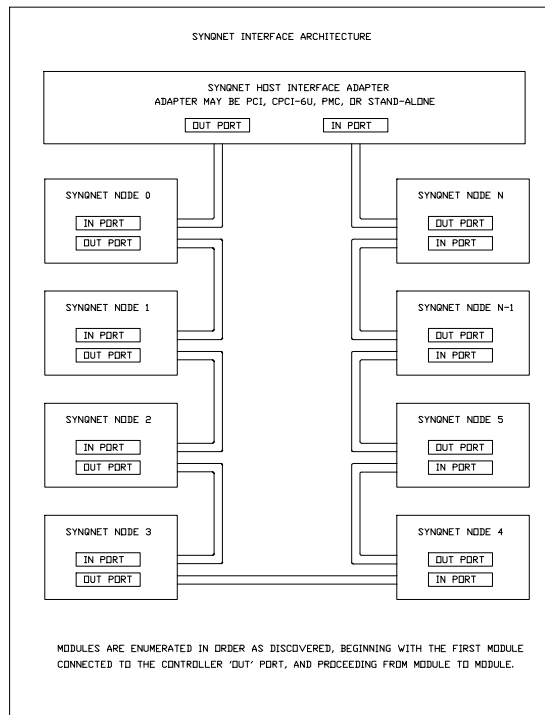


FIGURE 1 – SYNQNET NETWORK BLOCK DIAGRAM

The SynqNet cyclic rate can be approximated as shown in the following table. The table lists expected network performance based solely on network loading.



# OF SINGLE-AXIS NODES	CYCLIC RATE
4	48KHz
8	24KHz
12	16KHz
20	10KHz
24	8KHz
48	4KHz

Each TA805 Analog RIOB node occupies two axis of SynqNet network space. Each node contains eight analog inputs and four analog outputs, with the inputs assigned as eight per node, and the outputs distributed two per axis for a total of four per node.

Analog inputs are multiplexed into a common 16-bit serial A/D converter, and have an input range of -10V to +10Vdc. Analog outputs are driven from four individual serial D/A converters, and have an output range of -10V to +10Vdc.

The following block diagram shows the major functions of the TA805.

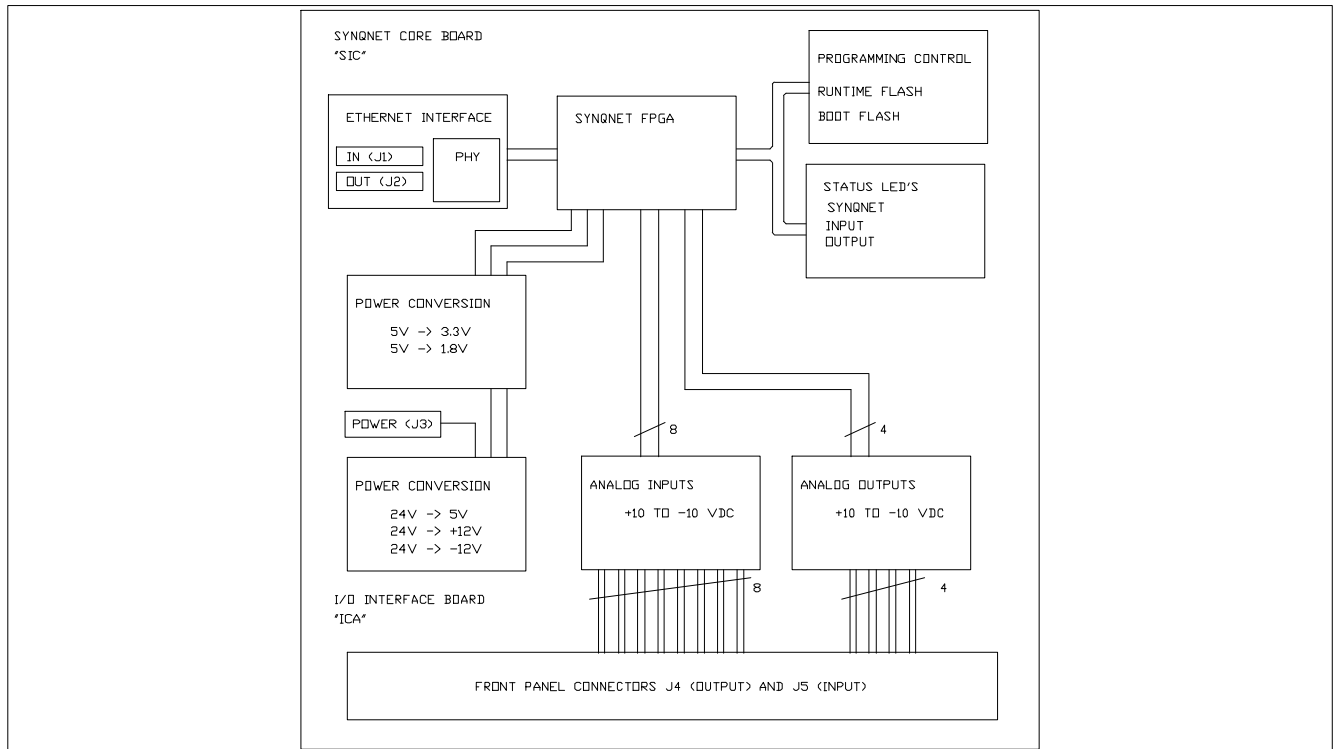


FIGURE 2 – TA805 FUNCTIONAL BLOCK DIAGRAM



4 FUNCTIONAL BLOCKS

This section gives greater detail on each of the functional blocks of the TA805 Analog RIOB. They are:

- SynqNet Network Interface
- SynqNet FPGA Core
- Analog Input Blocks
- Analog Output Blocks
- LED Status Indicators
- AMP FAULT Circuit
- SHUTDOWN Input Circuit

Each of these blocks is outlined in the following sections.

4.1 SYNQNET NETWORK INTERFACE

The RIOB Ethernet interface adheres to IEEE 802.3b Physical Ethernet Standard for 100BASE-TX. The conformance is physical layer only; all higher levels are SynqNet proprietary. The Ethernet interface is composed of the following components:

- Shielding RJ45 connectors, one for IN link and one for OUT link.
- 10/100BASE-T Magnetics
- 10/100BASE-TX Dual-Port Transceiver (PHY)
- Discrete filter components

The Broadcom physical layer interface (PHY) is programmed by the SynqNet FPGA, no direct user programming of the PHY is accessible.

The RIOB product family provides a cable support solution for use with RJ-45 cables. For additional details see Appendix B.

4.2 SYNQNET FPGA CORE

The SynqNet FPGA core is composed of the following major components:

- Xilinx XC2S200E FPGA
- Xilinx XC9572XL CPLD
- Atmel AT45DB021B Flash memories (1 for BOOT image, 1 for RUNTIME image)

The Xilinx FPGA controls all local execution of the RIOB module, directed by the SynqNet interface host controller. The Xilinx CPLD controls local programming of the RUNTIME Flash image, under network control.

Configuration data for the FPGA is stored as two unique images. The BOOT image is stored in one flash device, is programmed at the factory, and cannot be written or modified in the field. The RUNTIME image is stored in a second flash device, is programmed at the factory, but can be updated by the user via



the SynqNet interface. This gives the user the ability to update node firmware on all SynqNet nodes in his target system. After reset, the FPGA configuration data is normally loaded from the RUNTIME flash. If, during boot, the RUNTIME image is ever detected as corrupt or missing, the BOOT image is then loaded to allow reloading of RUNTIME images.

4.3 ANALOG INPUT BLOCKS

The analog input circuits on the RIOB are designed to allow the user to measure analog voltage inputs in a true differential fashion. Each multiplexed input block presents two input pins to the user, along with a shield ground pin. The following circuit block is representative of the analog inputs. Each pair of input pins on the front panel connector is routed to the right side of the schematic, nets ANALOG_IN_0+ and ANALOG_IN_0- are shown as an example.

- Unused input pin pairs will exhibit noise and are susceptible to crosstalk from adjacent channels if un-terminated. Grounding of unused input pins will eliminate signal coupling.
- The input voltage range is -10.0 to +10.0Vdc
- Input multiplexers and A/D are powered from +/- 15Vdc supplies
- The multiplexer input pins are internally protected to +/- 40Vdc continuous
- Fault-free input signal range is -12Vdc to +12Vdc
- Input gain is not selectable
- The input A/D converter is 16-bit
- Maximum continuous input pin current +/- 30mA

See Figure 3 for a representative schematic view of the input circuit. All eight input circuits are identical. Nets ANALOG_IN_0+ and ANALOG_IN_0- are connected directly to the J5 front plate connector.

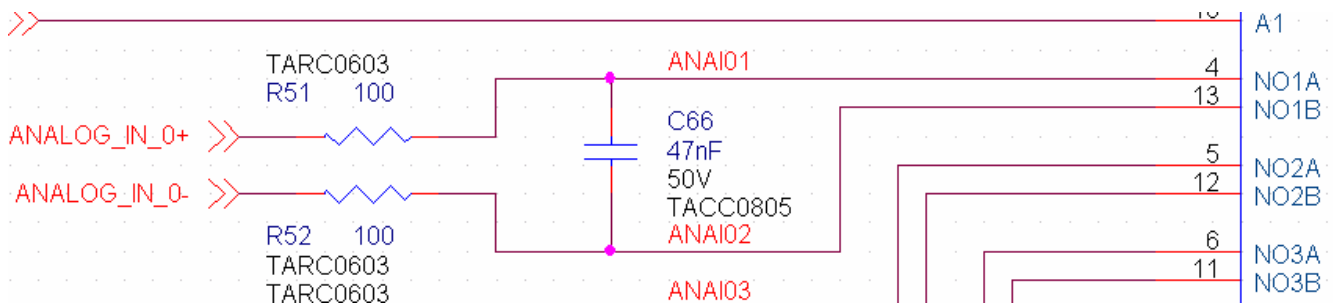


FIGURE 3 – ANALOG INPUT CIRCUIT



4.4 ANALOG OUTPUT BLOCKS

The analog output circuits on the RIOB are designed to allow the user to drive a -10Vdc to +10Vdc output voltage in a single-ended fashion. Each output block presents two output pins to the user, along with a shield ground pin.

Figures 4 and 5 following are representative of the analog output circuits. Serial DAC's are used in cascade, with the CMD DAC first in the chain and the AUX DAC second. All DAC's are controller directly by the SynqNet FPGA and are time-synchronized. Note that both DAC's associated with Axis 0 are shown in the first schematic fragment, and the output filter components for those two DAC's are shown in the second fragment. Each pair of connector analog output pins is routed to the right side of the second schematic fragment, examples shown are nets CMD_DAC_OUT_0+/- and AUX_DAC_OUT_0+/-.

The front panel connector (-) pins for all four DAC's are internally connected to analog ground.

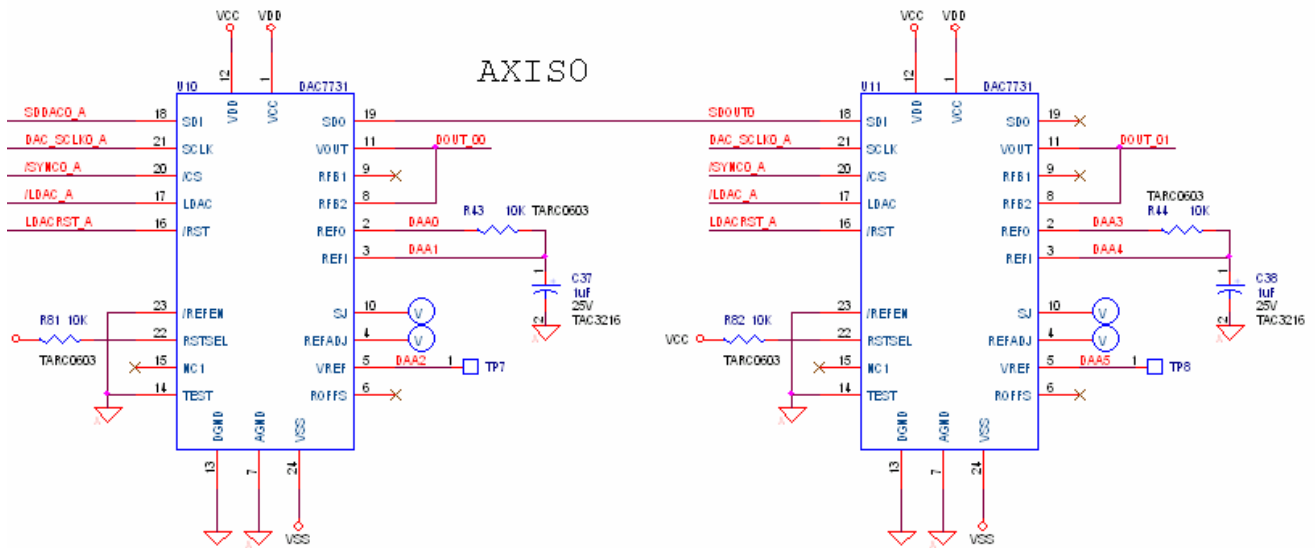


FIGURE 4– ANALOG OUTPUT DAC'S



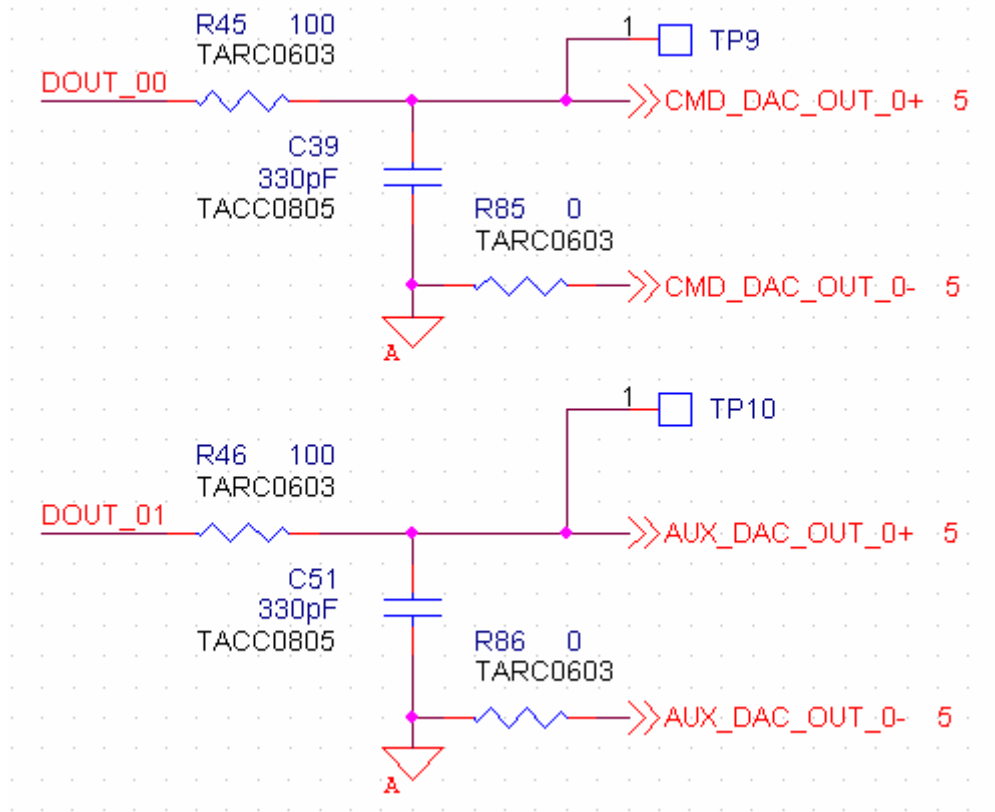


FIGURE 5 – ANALOG OUTPUT CIRCUIT FILTERS



4.5 LED STATUS INDICATORS

The RIOB module contains 6 status LED's which are all located on the front panel, next to J4. No status LED's are available for either analog input or analog output circuit states. These LED's are assigned as follows:

- D1 through D6 are status LED's for the SynqNet interface

These indicators are displayed pictorially in Figure 5 at the end of this section. The function of SynqNet status LED's D1 through D6 is as follows:

LED	Name	Color	Meaning when on	Controlled by	Mode
D1	STATUS	Blue	FPGA boot successful	FPGA	Blinking
D2	NODE	Green	Node state	FPGA	Blinking
D3	REPEAT	Green	Repeater ON	FPGA	Blinking
D4	IN ACT	Green	Link active	PHY	On
D5	OUT ACT	Green	Link active	PHY	On
D6	ALARM	Red	Node alarm exists	FPGA	On

D1, D2, D3, and D6 are used to indicate normal node status as follows:

Node state	STATUS Blue (D1)	NODE Green (D2)	REPEAT Green (D3)	ALARM Red (D6)
Unpowered	OFF	OFF	OFF	OFF
Reset	OFF	OFF	OFF	OFF
Undiscovered	BLINK .37 Hz	BLINK (1)	OFF	ON
Discovered	BLINK .75 Hz	BLINK (1)	OFF	ON
SYNQ	ON	ON	ON or OFF (3)	OFF
SYNQ lost	BLINK 1.5 Hz	BLINK (2)	BLINK (4)	ON

- (1) Blinks in same phase as **STATUS**
- (2) Blinks in opposite phase of **STATUS**
- (3) On if not node N-1, otherwise off
- (4) Off if node 0, otherwise blink in same phase as **STATUS**

The LEDs depend only on FPGA and network states. Note that in a fully-cabled network with all nodes in SYNC, the normal state of nodes 0 through node n-1 is to have **STATUS**, **NODE**, **REPEAT**, **IN ACT**, and **OUT ACT** continuously on. If the node is node N (the last node in a ring or string with more than one node) then **REPEAT** & **OUT ACT** should be off.



RIOB		
STATUS	BLUE	D1
NODE	GREEN	D2
REPEAT	GREEN	D3
IN ACT	GREEN	D4
OUT ACT	GREEN	D5
ALARM	RED	D6

FIGURE 6 – PANEL VIEW OF LED STATUS INDICATORS

4.6 AMP FAULT INPUT CIRCUIT

One additional source of error condition is AND'd into the Axis 0 AMP FAULT chain as seen by the FPGA. This source is:

SynqNet Module over Temperature (MT)

A solid-state temperature sensor is used to detect the internal temperature of the module. The sensor is located in the airflow path common to the FPGA. This sensor will be activated when the internal temperature of the module exceeds 72°F (22.2°C). This temperature sensor can be defeated from the amplifier chain as a manufacturing option. Contact Trust Automation for additional details.

4.7 SHUTDOWN INPUT CIRCUIT

The RIOB implements a method for the user to initiate a node disable from an external source. This is done using the SHUTDOWN+ and SHUTDOWN- pins on the OUTPUT connector J4. Assertion (bias) of the SHUTDOWN input will create a node alarm.

The SHUTDOWN+ pin (pin 25) and the SHUTDOWN- pin (pin 26) are connected to the anode and cathode legs (respectively) of an OPTO-isolator, limited with a 5.11K resistor. Thus the user can elect to bias the OPTO input circuit as a high-side switch or a low-side switch. Bias must be applied externally, using pin 16 (ISO24V) and one of the isolated ground return pins.

- If the OPTO input is disconnected or otherwise not biased, the output stage of the OPTO is off, the high level signal from the OPTO output stage is inverted and seen by the FPGA as a LOW, or inactive input.



- If the OPTO input is biased on, the output stage of the OPTO is on, the low level signal from the OPTO output stage is inverted and seen by the FPGA as a HIGH, or active input. A HIGH input to the FPGA means DISABLE the node.

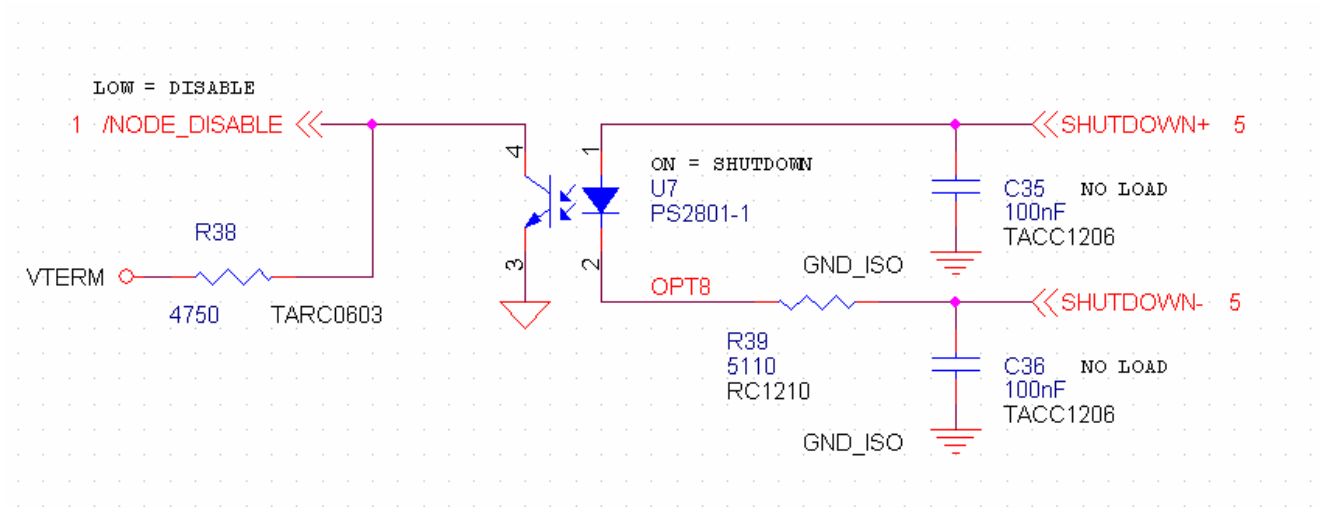


FIGURE 7 – SHUTDOWN INPUT CIRCUIT



4.7 AMPLIFIER ENABLE OUTPUT CIRCUITS

The RIOB implements OPTO-isolated output circuits for user with the DAC outputs. Each axis of the RIOB has an associated command and auxiliary DAC. The output enable associated with each axis can be used to provide simple, velocity-based drive control.

The output enable circuit is an active-low output that is configured to drive a 5V input to an amplifier. See Figure 8 for circuit details.

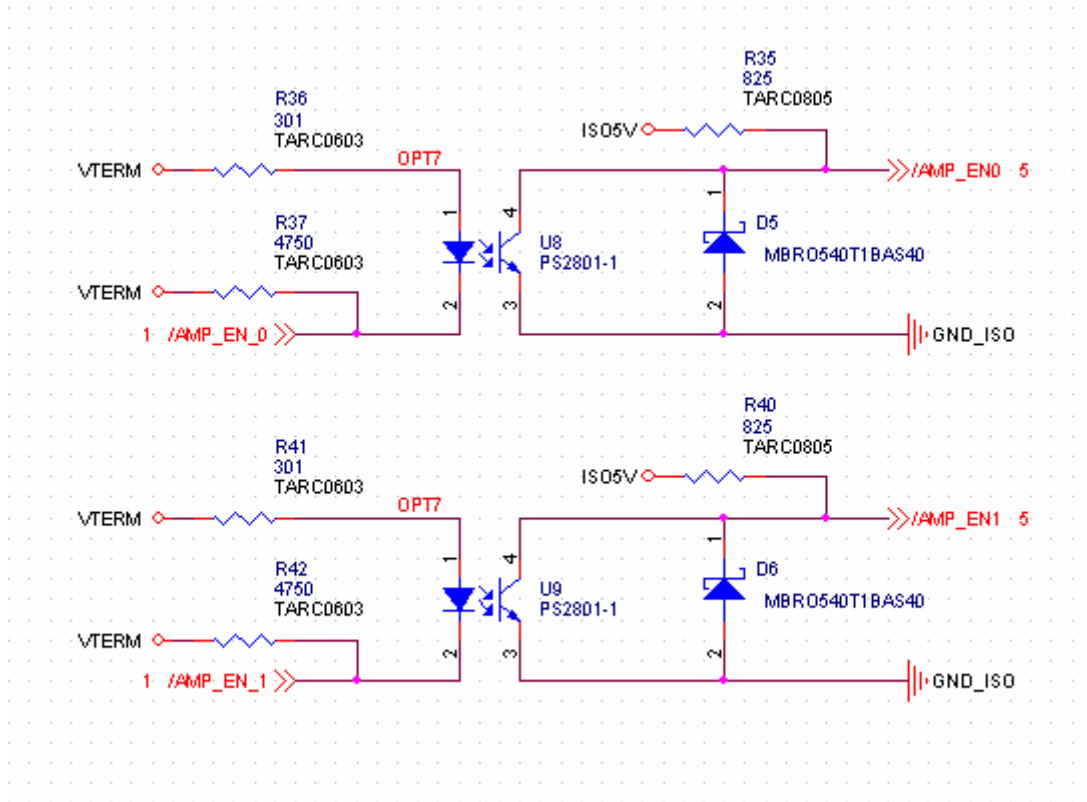


FIGURE 8 – AMP ENABLE OUTPUT CIRCUITS



5 CONNECTORS

The RIOB contains several panel connectors for external connections. These are designated as follows:

- J1 – SynqNet Interface IN connector
- J2 – SynqNet Interface OUT connector
- J3 – 24VDC power inlet connector
- J4 – Analog OUT connector
- J5 – Analog IN connector

Each connector type and style is described in additional detail in the following sections.

5.1 SYNQNET INTERFACE IN CONNECTOR (J1)

The SynqNet IN J1 connector is located on the bottom angled edge of the RIOB module. The connector is an RJ45 style connector, is labeled as 'IN', and is the RJ45 connector closest to the front (DB connectors) of the module. The board mounted connector is a Molex 85504-0001. Note that the Molex 85504 connector provides connectivity for shielded Ethernet cables. Shielded cables are recommended for the SynqNet interface but are not required. A representative mating shielded connector could be Molex 95043 Family or equivalent.

5.2 SYNQNET INTERFACE OUT CONNECTOR (J2)

The SynqNet OUT J2 connector is also located on the bottom angled edge of the RIOB module. The connector is an RJ45 style connector, is labeled as 'OUT', and is the RJ45 connector closest to the rear (bulkhead flange) of the module. The board mounted connector is a Molex 85504-0001. Note that the Molex 85504 connector provides connectivity for shielded Ethernet cables. Shielded cables are recommended for the SynqNet interface but are not required. A representative mating shielded connector could be Molex 95043 Family or equivalent.

5.3 POWER INLET CONNECTOR (J3)

The power inlet J3 connector is located on the bottom of the RIOB SynqNet module. The board mounted connector is a Phoenix Contact Combicon™ family P/N 17 76 50 8, the external mating connector is a Phoenix Contact P/N 17 77 98 9, and is supplied with every RIOB module. Note that the Phoenix Contact connector accepts wires sizes between 12 and 24 AWG. The RIOB inlet power required is 24VDC +/- 3VDC. The RIOB inlet power path is protected with a 3A PTC and a 3A blocking diode.

The RIOB provides isolated 24Vdc to the user via front panel connectors J4 (pin 39) and J5 (pins 31-42). Note this 24V source is isolated from the inlet supply with a 1.5A resettable circuit protection device (PTC).

Note: If the RIOB input voltage is 24.0Vdc, the isolated 24VDC provided to the user on front panel connectors J4 and J5 will be between 23.2 and 23.4 Vdc. This is due to the voltage drop of the protection device and blocking diode.



5.4 ANALOG OUTPUT CONNECTOR (J4)

The J4 connector is a 26 pin female high density D-Sub connector. The connector used in the RIOB is a Kycon K66-B26S-N. A representative mating connector is NORCOMP 180-026-102-001. A representative backshell kit is NORCOMP 977-015-020-121.

The following tables detail the pin assignments and definitions of J4:

RIOB Physical Connector		ICA R0
View		
PWS	6/20/2003	

RIOB - J4					
ANALOG OUT Physical View					
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	CDO0+	10	AORTN	19	CDO0-
2	ADO0+	11	AORTN	20	ADO0-
3	AORTN	12	AORTN	21	AORTN
4	CDO1+	13	AORTN	22	CDO1-
5	ADO1+	14	AORTN	23	ADO1-
6	AORTN	15	AORTN	24	AORTN
7	AE0	16	LOC24V	25	/SHUTDOWN+
8	RTN	17	RTN	26	/SHUTDOWN-
9	AE1	18	FRAME		

Table 1 – J4 Pin Assignments



PIN	Definition
1	CMD DAC 0 Positive Output
2	AUX DAC 0 Positive Output
3	Load R22 for FRAME, load R25 for GND_ISO
4	CMD DAC 1 Output
5	CMD DAC 1 Return
6	Load R22 for FRAME, load R25 for GND_ISO
7	Amplifier Enable 0 Output (active low output)
8	Isolated GND return
9	Amplifier Enable 1 Output (active low output)
10	Load R22 for FRAME, load R25 for GND_ISO
11	Load R22 for FRAME, load R25 for GND_ISO
12	Load R22 for FRAME, load R25 for GND_ISO
13	Load R22 for FRAME, load R25 for GND_ISO
14	Load R22 for FRAME, load R25 for GND_ISO
15	Load R22 for FRAME, load R25 for GND_ISO
16	Local 24V
17	Isolated GND return
18	FRAME GND
19	CMD DAC 0 Return
20	AUX DAC 0 Return
21	Load R22 for FRAME, load R25 for GND_ISO
22	AUX DAC 1 Output
23	AUX DAC 1 Return
24	Load R22 for FRAME, load R25 for GND_ISO
25	/SHUTDOWN+
26	/SHUTDOWN-

Table 2 – J4 Pin Definitions



5.5 ANALOG INPUT CONNECTOR (J5)

The J5 connector is a 26 pin male high density D-Sub connectors. The connector used in the RIOB is a Kycon K66-B26P-N. A representative mating connector is NORCOMP 180-026-202-001. A representative backshell kit is NORCOMP 977-015-020-121.

The following tables detail the pin assignments and definitions of J5:

RIOB Physical Connector View		ICA R0
PWS	6/20/2003	

RIOB - J5					
ANALOG IN Physical View					
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	IN0+	10	FRAME	19	IN0-
2	IN1+	11	FRAME	20	IN1-
3	IN2+	12	FRAME	21	IN2-
4	IN3+	13	FRAME	22	IN3-
5	IN4+	14	FRAME	23	IN4-
6	IN5+	15	FRAME	24	IN5-
7	IN6+	16	FRAME	25	IN6-
8	IN7+	17	FRAME	26	IN7-
9	FRAME	18	FRAME		

Table 3 – J5 Pin Assignments



PIN	Definition
1	Analog Input 0 Positive
2	Analog Input 1 Positive
3	Analog Input 2 Positive
4	Analog Input 3 Positive
5	Analog Input 4 Positive
6	Analog Input 5 Positive
7	Analog Input 6 Positive
8	Analog Input 7 Positive
9	FRAME
10	Load R21 for GND_ISO, load R23 for FRAME
11	Load R26 for ISO5V, load R24 for FRAME
12	Load R21 for GND_ISO, load R23 for FRAME
13	Load R26 for ISO5V, load R24 for FRAME
14	Load R21 for GND_ISO, load R23 for FRAME
15	Load R26 for ISO5V, load R24 for FRAME
16	Load R21 for GND_ISO, load R23 for FRAME
17	Load R26 for ISO5V, load R24 for FRAME
18	FRAME
19	Analog Input 0 Negative
20	Analog Input 1 Negative
21	Analog Input 2 Negative
22	Analog Input 3 Negative
23	Analog Input 4 Negative
24	Analog Input 5 Negative
25	Analog Input 6 Negative
26	Analog Input 7 Negative

Table 4 – J5 Pin Definitions



6 SPECIFICATIONS

This section lists the mechanical, electrical, and environmental specifications for the TA805 RIOB module family.

6.1 MECHANICAL DIMENSIONS

This section details the basic mechanical dimensions of the TA805 Digital RIOB modules. Overall size and mounting locations are provided.

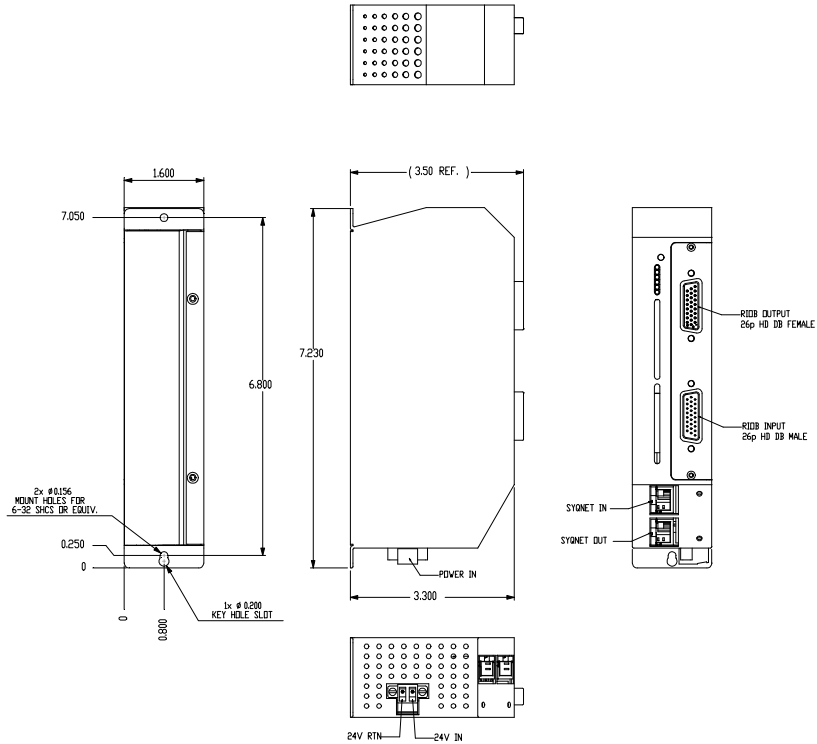


FIGURE 9 – MECHANICAL DIMENSIONS



6.2 ELECTRICAL REQUIREMENTS

INPUT POWER

The RIOB requires the following input power based on internal and external usage. Internal usage is consumed within the module by internal circuitry. External usage is dissipated external to the module via user components connected to the various power source and return pins on J4 and J5. External power usage is not considered part of the thermal cooling requirements for the module.

- Input Voltage: 24V +/- 3.0VDC, ripple/noise less than 0.3VDC peak
- Input Current 325mA maximum, 190mA typical

- Internal Power 5.4W maximum
- External 24V 2.4W maximum (100mA maximum)
- Total Power 7.8W maximum

USER POWER

The RIOB can provide 24VDC power for bias of the SHUTDOWN input circuit on the J4 front panel connectors. Available on J4 pin 16, this power pin is limited to 100mA maximum load.

ETHERNET

Ethernet Input/Output IEEE 802.3b IEEEBase100-TX (physical layer only)
100Base-T CAT 5 or better cabling required
Shielded cables recommended but not required
100m length per link (max)

SIGNAL REQUIREMENTS

Shutdown Input 24VDC +/- 3.0VDC @ 5 mA (min)
Analog Inputs -10.0Vdc to +10.0Vdc full-scale input range (30mA maximum)
Analog Outputs -10.0Vdc to +10.0Vdc full-scale output range (10mA maximum)



6.3 ENVIRONMENTAL

OPERATING TEMPERATURE:	0°C (min) to 50°C (max)
TEMPERATURE CHANGE	10°C per hour (max)
HUMIDITY	0% to 95% Relative Humidity, non-condensing
VIBRATION	1.5mm (0.060") P-P sinusoidal
SHOCK	30g half sine shock 11msec individual axis

Exceptions to the product vibration and shock are Ethernet connectors. The specifications for the Molex 85504-0001 modular jacks used on the production RIOB modules are as follows:

MFGR Spec:	Molex PS-85505 FCC Part 68, Subpart F
Vibration:	1.5mm (0.060") P-P 10-55-10 Hz sweep per minute 2 hours in each X-Y-Z axis
Shock:	No discontinuities greater than 1 usec 50g three sawtooth waveform shocks in each X-Y-Z axis No discontinuities greater than 1 usec
Mating Family:	95043 Series

Note that the RIOB product family provides for the use of cable support brackets with Ethernet cables plugged into connectors J1 and J2. See the Appendix B for additional details.



6.4 COOLING REQUIREMENTS

The TA805 RIOB can dissipate up to 5.4W internally. Convective cooling requires mounting the RIOB vertically, as shown below. 1.5 inches of clearance is required both above and below the module for convective cooling airflow.

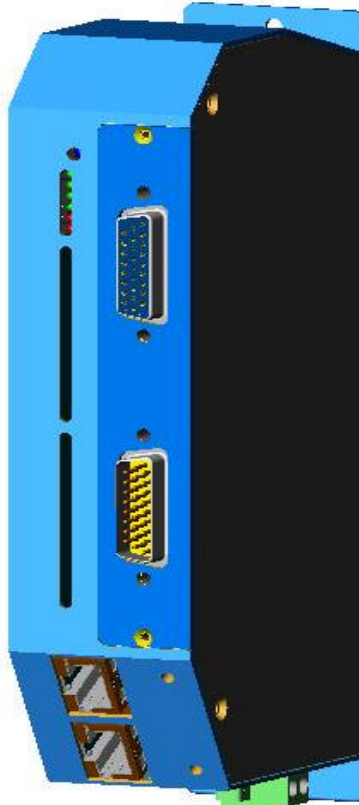


FIGURE 10 – MOUNTING VIEW

For special mounting considerations or environments, internally mounted fan-forced cooling is available as a manufacturing option. For available product options see Appendix B. When the internal forced cooling is used the RIOB module may be mounted either horizontally or vertically. It should not be mounted in an inverted orientation (meaning with J3 on top).



7 SOFTWARE

REQUIRED SOFTWARE LEVELS AND REVISIONS

The RIOB requires specific revision levels of software in order to function correctly. Software revisions required from MEI are as follows:

MEI XMP Software: **TBD**

MEI Host Firmware: **TBD**

RIOB FPGA Runtime Version: **TBD**

APPENDIX A – POWER INLET CIRCUIT BLOCK

The following circuit block shows the circuit protection elements in the power inlet stage. This is provided for reference only.

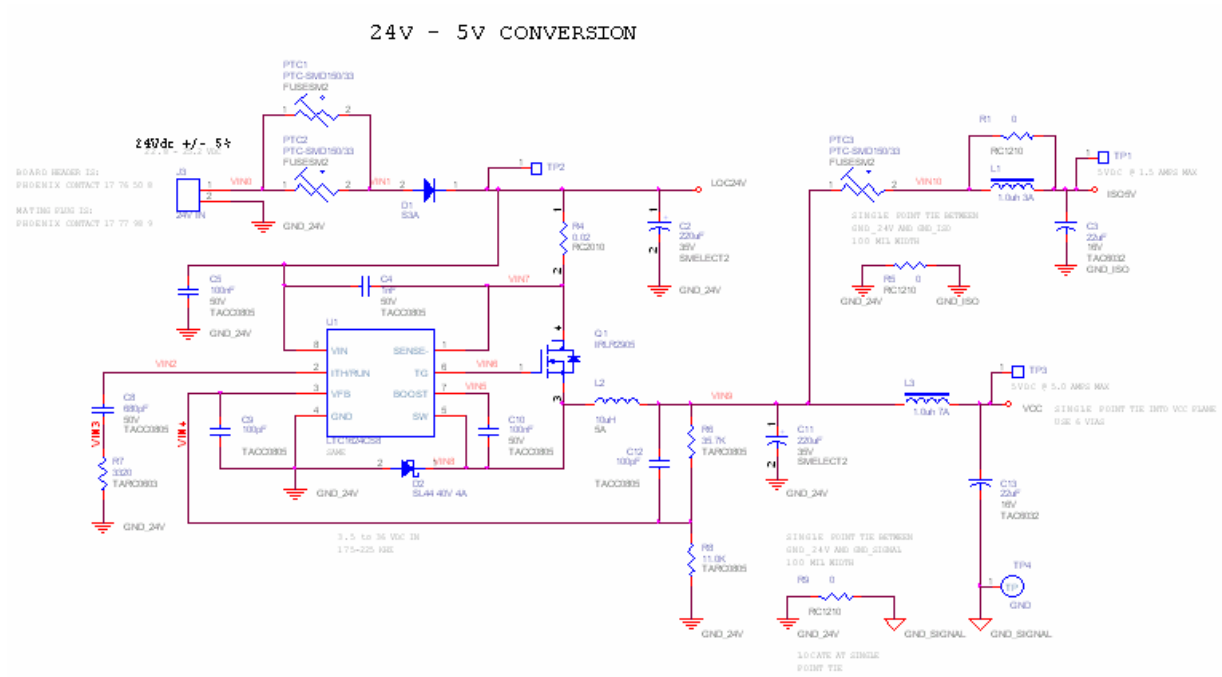


FIGURE 11 – POWER INLET CIRCUIT



APPENDIX B – PRODUCT OPTIONS

Any TA805 module may be ordered with an Ethernet cable clamping option. When attached, this bracket clamps the Ethernet cables in place, minimizing movement of the Ethernet cables relative to the module. The cable clamping option is ordered as:

P/N: **TBD**

Any TA805 module may be ordered with a cooling fan option. This 2.0 CFM fan, installed internally to the module during manufacturing, is recommended if horizontal mounting is expected. When ordered on the same purchase order as TA805 modules, fan assemblies are integrated into the purchased modules prior to shipment. Fan assemblies can be ordered separately from TA805 modules. The fan option is ordered as the following P/N (on a separate line item on the same PO as the RIOB):

P/N: **TBD**

APPENDIX C – HARDWARE ERRATA

Hardware changes occurred during the development of the TA805 RIOB. These changes are detailed below.

- Prototype RIOB modules (containing SIC PCB-0804-01 Rev 0) were shipped to customers and beta-sites with Ethernet connectors that would not guarantee isolation between the connector shields and the chassis. This was revised after the first round of prototypes.
- Prototype RIOB modules used AMP 406541-1 (or -5) for the Ethernet connectors. After the first prototype run the connectors were changed to Molex 85504-0001.



APPENDIX D – CONTACT INFORMATION

Do you have hardware Questions?

Any hardware questions regarding use and operation of the Trust Automation TA805 Digital RIOB family of products should be directed to:

Trust Automation, Incorporated
205 Suburban Road
San Luis Obispo, CA 93401

Corporate Office Telephone: (805) 544-0761
Corporate Office Facsimile: (805) 544-4621

Corporate Website: www.trustautomation.com

Email: support@trustautomation.com

Do you have software Questions?

Any questions regarding use and operation of MEI XMP software with the TA805 RIOB family of Digital I/O products should be directed to:

Motion Engineering, Incorporated
33 South La Patera Lane
Santa Barbara, CA 93117-3214

Corporate Office Telephone: (805) 681-3300
Corporate Office Facsimile: (805) 681-3311

Corporate Website: www.motioneng.com

Email: info@motioneng.com

Additional information regarding the SynqNet Interface Standard can be found at:

http://www.synqnet.org/tech_library.html



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