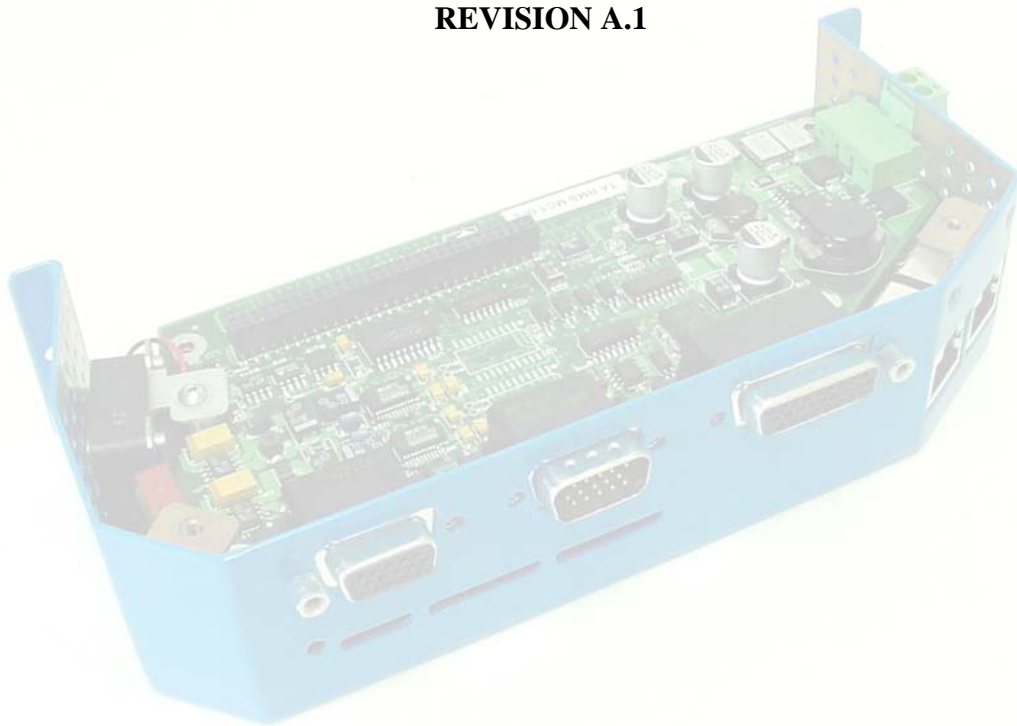


SYNQNET® REMOTE MOTION BLOCKS TA801 AND TA802

REVISION A.1



REVISION HISTORY

Date	Revision	Description	Author
11/07/2003	Rev 0	Initial draft of Manual	Pat Scrivner
11/13/2003	Rev 0.1	Graphic updates	Pat Scrivner
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1 SCOPE

This manual documents the function and usage of the Trust Automation TA801 and TA802 SynqNet® Remote Motion Block (RMB) series of products. These products are used in SynqNet-based networked motion control systems to provide time-correlated input and output functions at SynqNet update rates. It is the goal of this manual to provide the user with information sufficient to support setup and normal use of these products.

This manual pertains to the following TA801 and TA802 products:

- TA801-D01 RMB, 1-Axis, Dual DAC, High Density DB connectors
- TA801-E01 RMB, 1-Axis, Single DAC, High Density DB connectors
- TA801-F01 RMB, 1-Axis, Stepper, High Density DB connectors
- TA801-D21 RMB, 1-Axis, Dual DAC, High Density DB connectors, with Fan
- TA801-E21 RMB, 1-Axis, Single DAC, High Density DB connectors, with Fan
- TA801-F21 RMB, 1-Axis, Stepper, High Density DB connectors, with Fan

- TA802-D01 RMB, 2-Axis, Dual DAC, High Density DB connectors
- TA802-E01 RMB, 2-Axis, Single DAC, High Density DB connectors
- TA802-F01 RMB, 2-Axis, Stepper, High Density DB connectors
- TA802-D21 RMB, 2-Axis, Dual DAC, High Density DB connectors, with Fan
- TA802-E21 RMB, 2-Axis, Single DAC, High Density DB connectors, with Fan
- TA802-F21 RMB, 2-Axis, Stepper, High Density DB connectors, with Fan

***NOTE. FAN OPTIONS CURRENTLY UNRELEASED. CONTACT TRUST AUTOMATION SALES FOR ADDITIONAL INFORMATION.**

2 DEFINITIONS

Throughout this manual, various terms and acronyms are used in discussion of SynqNet® and the TA801/TA802 RMB product family. Definition of those most commonly used follows:

- AIO Analog I/O
- AMP Amplifier or drive for motor
- Axis Reference to all components relating to a single axis of motion
- CAT5 Category 5 cabling Ethernet cabling
- DIO Digital I/O
- DTS Dynamic Transconductance Select
- Ethernet IEEE 802.3b Physical Ethernet Standard for 100BASE-TX
- Flash Non-volatile memory or memory device
- FPGA Field Programmable Gate Array
- I/O Input/Output, generally refers to bitwise control
- LED Light Emitting Diode, used as status indicators
- Module SynqNet Node
- MT Module Over-Temperature condition
- Node Means 'slave-mode' and not the controller
- PHY Ethernet physical layer interface device
- PTC Positive Temperature Coefficient
- RING SynqNet network topology with return link
- RIOB Remote I/O Block, component of SynqNet network
- RMB Remote Motion Block, component of SynqNet network
- RT Relay Over-Temperature condition
- SSR Solid State Relay
- STRING SynqNet network topology without return link
- SynqNet® A 100Mbit, full duplex motion control network

TRADEMARKS:

SynqNet® - Motion Engineering, Incorporated

All other trademarks are the properties of their respective companies.

3 DESCRIPTION

The TA801/TA802 RMB products communicate with a centralized, motion control network via the SynqNet® standard interface developed by Motion Engineering Inc. SynqNet is an all-digital motion control interface for connections between motion controllers and drives. The physical layer of SynqNet is based on IEEE 802.3 standards for 100Base-X, the physical layer of Ethernet. The data link and application layers of SynqNet were designed by MEI. The 100Base-TX media system is based on specifications published in the ANSI TP-PMD physical media standard. The 100Base-TX system operates over two pairs of wires, one for receive data signals and one for transmit data signals. SynqNet is strictly master-slave in concept. There is no peer-to-peer communication. SynqNet is not compatible with Ethernet hubs or switches.

SynqNet networks can exist as one of two topologies, either 'RING' or 'STRING'. The ring topology provides the return link from the last node, the string topology does not. Ring networks are fault-tolerant, self-healing (within two servo cycles) and implement two full-duplex 100Mbit channels from the nodes to the controller. String networks are not fault-tolerant, and consist of one full-duplex 100Mbit channel from the nodes to the controller. The interface is made up of an Ethernet hardware layer, with redundant connections. Node link connections are electrically isolated at both ends. The inter-node cabling used is shielded CAT5 100BaseT or better. (Shielding is recommended, but not required.) See Figure 1 for a representative example of a RING network with enumerated node ID's.

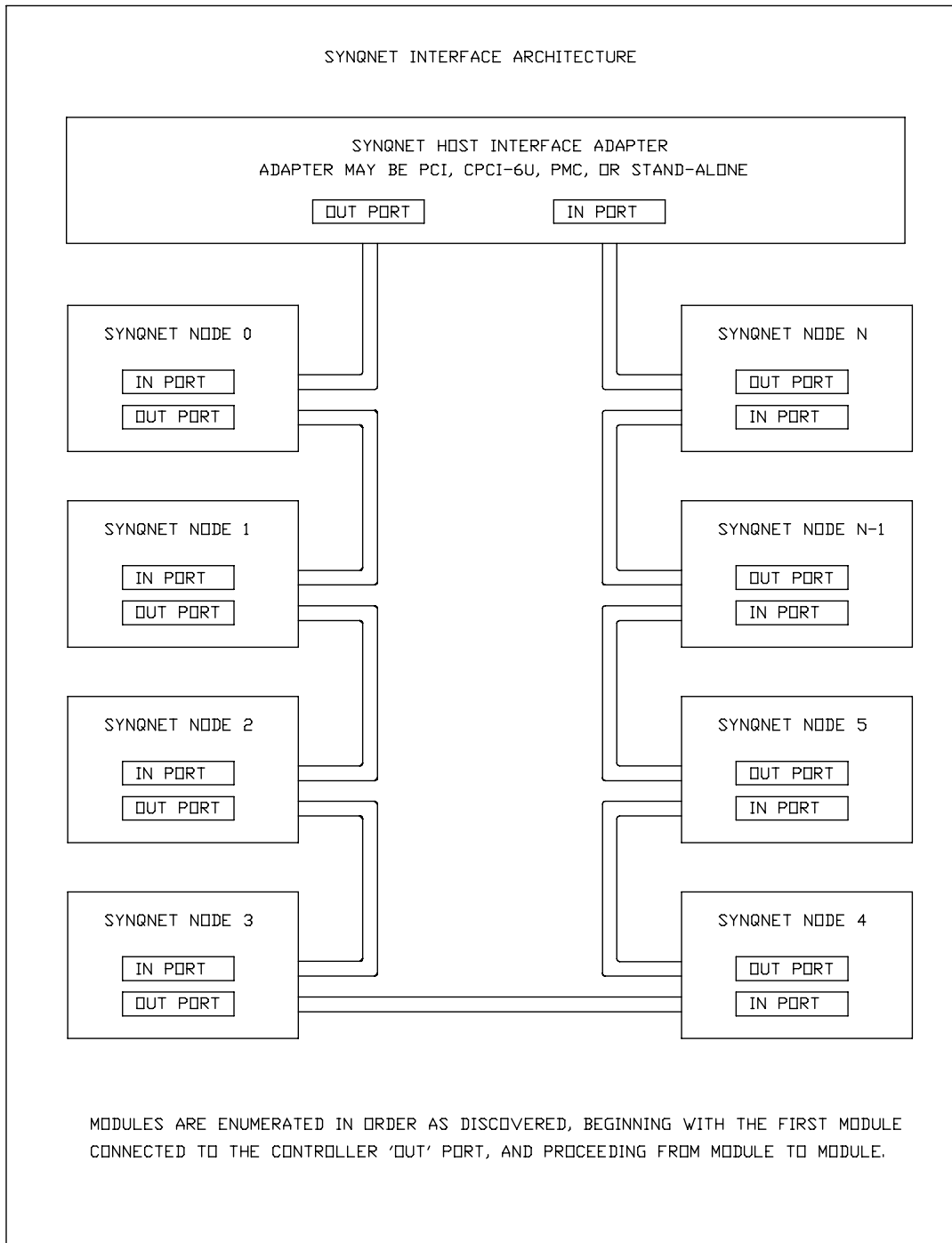


FIGURE 1 – SYNQNET NETWORK BLOCK DIAGRAM

SynqNet network cyclic update rates can be approximated as shown in Table 1. The table lists expected performance based solely on network loading.

# OF SINGLE-AXIS NODES	CYCLIC RATE
4	48KHz
8	24KHz
12	16KHz
20	10KHz
24	8KHz
48	4KHz

Table 1 – Cyclic Update Rate

Each TA801 RMB node occupies one axis of SynqNet network space. Each TA802 RMB node occupies two axis of SynqNet network space.

Each TA801 or TA802 axis contains input and output circuitry specific to control motor, amplifier, and sensor interfaces normally found on servo and stepper controlled motion axes. The interface functions found on each axis are:

- Amplifier Enable Output
- Amplifier Fault input
- DTS control outputs (2 outputs)
- Motor Brake control output
- Command DAC (+/- 10V)
- Auxiliary DAC (+/- 10V)
- Encoder input channel (A,B,Z)
- Hall input channel (A,B,C)
- Home input
- Positive limit input
- Negative limit input
- 24V 500mA output (user defined)
- 24V OPTO input (user defined)
- Capture input
- STEP and DIR RS-422 outputs
- User RS-422 outputs (2)
- SHUTDOWN input

Figure 2 shows the major functional blocks of the TA801 and TA802 products. Note that the difference between the TA801 and TA802 is that the TA801 does not have axis 1 components installed.

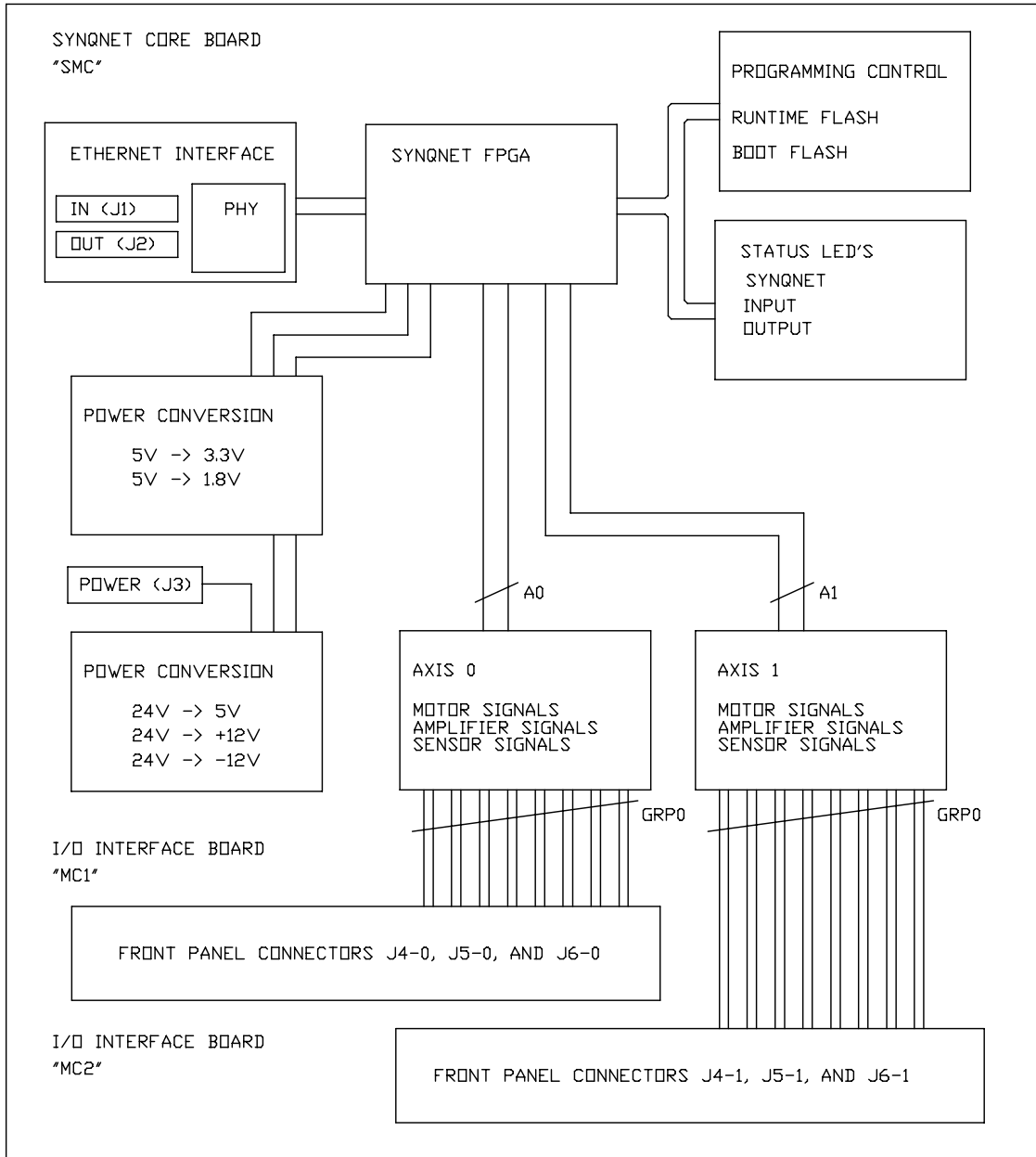


FIGURE 2 – TA801 AND TA802 FUNCTIONAL BLOCK DIAGRAM

4 FUNCTIONAL BLOCKS

This section gives greater detail on each of the functional blocks of the TA801 and TA802 RMB products. The functional blocks discussed are:

- SynqNet Network Interface
- SynqNet FPGA Core
- Amplifier Enable Output
- Brake Output
- Amplifier Fault Input
- Shutdown Input
- Analog Outputs
- Encoder Inputs
- Hall Sensor Inputs
- Home and Limit Sensor Inputs
- User Input
- User Output
- Capture Input
- LED Status Indicators
- DTS Outputs
- Stepper Transceiver Outputs

The specific I/O functions present on the different TA801 models are listed in the following table:

Function	TA801-D01		TA801-E01		TA801-F01	
	Axis 0	Axis 1	Axis 0	Axis 1	Axis 0	Axis 1
Amp Enable 0 Output	Yes	No	Yes	No	Yes	No
Brake 0 Output	Yes	No	Yes	No	Yes	No
Amp Fault 0 Input	Yes	No	Yes	No	Yes	No
Shutdown Input	Yes	No	Yes	No	Yes	No
Command DAC Output	Yes	No	Yes	No	No	No
Auxiliary DAC Output	Yes	No	No	No	No	No
Encoder Inputs	Yes	No	Yes	No	Yes	No
Hall Inputs	Yes	No	Yes	No	Yes	No
Home Input	Yes	No	Yes	No	Yes	No
Positive Limit Input	Yes	No	Yes	No	Yes	No
Negative Limit Input	Yes	No	Yes	No	Yes	No
User Input	Yes	No	Yes	No	Yes	No
User Output	Yes	No	Yes	No	Yes	No
Capture Input	Yes	No	Yes	No	Yes	No
DTS Outputs	Yes	No	Yes	No	Yes	No
Stepper Outputs	Yes	No	Yes	No	Yes	No

The specific I/O functions present on the different TA802 models are defined in the following table:

Function	TA802-D01		TA802-E01		TA802-F01	
	Axis 0	Axis 1	Axis 0	Axis 1	Axis 0	Axis 1
Amp Enable 0 Output	Yes	Yes	Yes	Yes	Yes	Yes
Brake 0 Output	Yes	Yes	Yes	Yes	Yes	Yes
Amp Fault 0 Input	Yes	Yes	Yes	Yes	Yes	Yes
Shutdown Input	Yes	Yes	Yes	Yes	Yes	Yes
Command DAC Output	Yes	Yes	Yes	Yes	No	No
Auxiliary DAC Output	Yes	Yes	No	No	No	No
Encoder Inputs	Yes	Yes	Yes	Yes	Yes	Yes
Hall Inputs	Yes	Yes	Yes	Yes	Yes	Yes
Home Input	Yes	Yes	Yes	Yes	Yes	Yes
Positive Limit Input	Yes	Yes	Yes	Yes	Yes	Yes
Negative Limit Input	Yes	Yes	Yes	Yes	Yes	Yes
User Input	Yes	Yes	Yes	Yes	Yes	Yes
User Output	Yes	Yes	Yes	Yes	Yes	Yes
Capture Input	Yes	Yes	Yes	Yes	Yes	Yes
DTS Outputs	Yes	Yes	Yes	Yes	Yes	Yes
Stepper Outputs	No	No	No	No	Yes	Yes

4.1 SYNQNET NETWORK INTERFACE

The TA801 and TA802 RMB Ethernet interface adheres to IEEE 802.3 Physical Ethernet Standard for 100BASE-TX. The conformance is physical layer only; all higher levels are SynqNet proprietary. The Ethernet interface is composed of the following major components:

- Molex 85504 shielding modular (RJ-45) connectors, one for IN link and one for OUT link.
- Pulse H1102 10/100BASE-T Magnetics
- Broadcom BCM5222 10/100BASE-TX Dual-Port Transceiver
- Discrete filter components

The Broadcom physical layer interface (PHY) is programmed by the SynqNet FPGA, no direct user programming of the PHY is accessible.

The SynqNet network specification provides for use of RJ-45 style modular Ethernet connectors or Micro-D Subminiature (MDSM) connectors. The Trust Automation SynqNet product families use only modular connectors to provide a low-cost solution. The RMB product family provides a cable support solution for use with Ethernet RJ-45 cables. For additional details see Appendix A.

4.2 SYNQNET FPGA CORE

The SynqNet FPGA core controls all local execution of the RMB module, directed by the SynqNet host interface controller. The core controls local in-situ programming of the RUNTIME Flash image, under network control.

Configuration data for the FPGA is stored as two unique images. The BOOT image is stored in one flash device. This device is programmed at the factory, and cannot be written or modified in the field.

The RUNTIME image is stored in a second flash device, and is programmed by the user via the SynqNet network interface. The user must select and program the RUNTIME image to match his specific network software requirements. This gives the user the ability to update and maintain node firmware on all SynqNet nodes in his target system. After reset, the FPGA configuration data is normally loaded from the RUNTIME flash. If, during boot, the RUNTIME image is detected as corrupt or missing, the BOOT image is then loaded to allow the user to reprogram the RUNTIME image via the SynqNet network.

Node-specific hardware information is stored in an EEPROM located in the SynqNet core. Of interest to the user would be the Node type, serial number, and unique ID. This information allows the user to identify, via the SynqNet network, all node types present, and to identify any changes made to the network.

Please note that TA801 and TA802 RMB Modules are shipped without a FPGA Runtime image loaded. This provides the customer with the opportunity to assure that the Runtime image correct for his current network level can be loaded into the module after installation.

4.3 AMPLIFIER ENABLE OUTPUT

The RMB implements OPTO-isolated output circuits for amplifier control. The output enable associated with each axis can be programmed to provide an event-driven amplifier control signal.

The output enable circuit is an active-on optically isolated output that is configured to connect both collector (AMP_EN_0+) and emitter (AMP_EN_0-) to the J5 connector. This provides a path for external bias to an amplifier's enable input pin. Amplifier input circuit configurations vary. The user will need to inspect the input configuration of the specific amplifier used in order to determine the correct bias configuration. The provision of collector and emitter outputs allows the user to configure the control as high-side or low-side, thus creating either active-high or active-low outputs. The suggested value for a current limiting resistor for 5V logic is 825 ohm, and for 24V logic is 5.11Kohm. Collector current in the output transistor must be limited to less than 50mA. Collector-to-emitter voltage must be limited to 80Vdc maximum forward, and 6Vdc maximum reverse. See Figure 3 for circuit details.

The AMP Enable circuits on axis 0 and axis 1 are identical, the description and Figure 3 apply equally to both axes. (Note that early revision RMB modules used a single-ended input model for axis 1. For additional information see Appendix B).

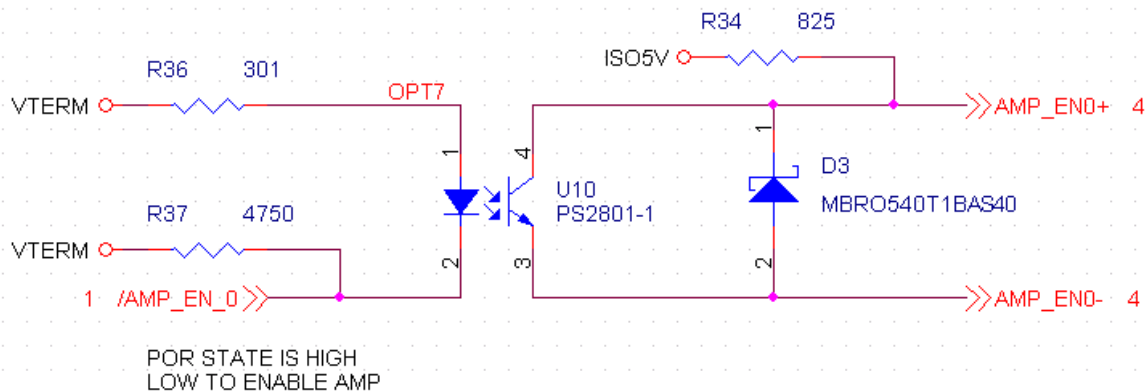


FIGURE 3 – AMPLIFIER ENABLE OUTPUT CIRCUIT

4.4 BRAKE OUTPUT

The RMB implements control for an external motor brake for each axis. The brake output associated with each axis can be SW programmed to be activated and deactivated driven by hardware events, and can be complementary with the output enable circuit. Brake delay is SW programmable.

The brake control pins on connector J4-0 and J4-1 consist of the control pin (J6 pin 8), and a dedicated return pin (J6 pin 9). The brake output driver circuit is both optically isolated and buffered using a high-current solid state relay (SSR) as a high-side switch. The brake output will be tri-state when the SSR driver is off. The brake output will be a low impedance path to internal isolated 24V (0.4 ohm maximum) when the SSR driver is on. The brake output states are controlled by hardware and FPGA logic as follows:

Hardware State	BRAKE SSR Output
During Power On	Off
During Hardware Reset	
During FPGA Configuration	
After FPGA Configuration	
After SW Brake Release	On

This circuit is designed to provide brake control for motors that require an energized 24V brake control signal to release the brake. Each SSR driver is rated for 500ma (maximum), and is thermally protected from over-current conditions. A SSR driver will disconnect and generate an AMP fault signal specific to the axis of control if it overheats. Other drivers are not affected. When the overheated SSR driver cools it will reconnect and the AMP fault signal will be removed. This cycle will continue until the source of the thermal fault is removed.

4.5 AMPLIFIER FAULT INPUT

The RMB can be programmed to generate a fault based on multiple types of input events. A fault usually generates a NODE_ALARM condition. One of these input events is an amplifier fault from either axis.

For axis 0 of the TA801 and TA802 RMB, the AMP FAULT input to the FPGA can be set active by one of the following conditions:

- Active high FAULT input from J5-0 pin 3
- SynqNet Module over Temperature (MT)
- BRAKE driver over Temperature (RT)
- USER OUT driver over temperature (RT)

For axis 1 of the TA802 RMB, the AMP FAULT input to the FPGA can be set active by one of the following conditions:

- Active high FAULT input from J5-1 pin 3
- BRAKE driver over Temperature (RT)
- USER OUT driver over temperature (RT)

These additional sources of error condition are AND'd into the specific axis amplifier fault input as seen by the FPGA. Note that the fault chain is a logical AND, a fault will exist until all sources are removed.

The external FAULT input for each axis is an optically isolated input on J5 pin3. The signal is active low, and the external driver must sink 5mA (min) at 0.8Vdc (max). See Figure 4 for input details.

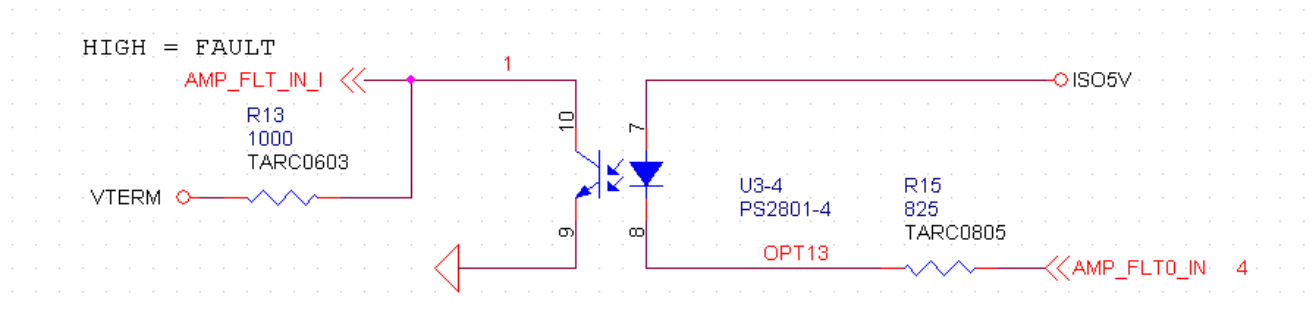


FIGURE 4 – AMP FAULT INPUT

Note that the external fault input is active by default. If the input is disconnected or is not biased, the FPGA will sense an active fault input. If the input is held low, the FPGA will not see a fault.

A Module Over-Temperature (MT) fault is generated only by axis 0 of the RMB. The MT fault is driven by a solid-state temperature sensor used to detect the internal temperature of the module. The sensor is located in the airflow path common to the FPGA. This sensor will be activated when the internal

temperature of the module exceeds 162°F (72°C). The MT temperature sensor can be defeated from the amplifier chain as a manufacturing option. See Figure 5. Contact Trust Automation for additional details.

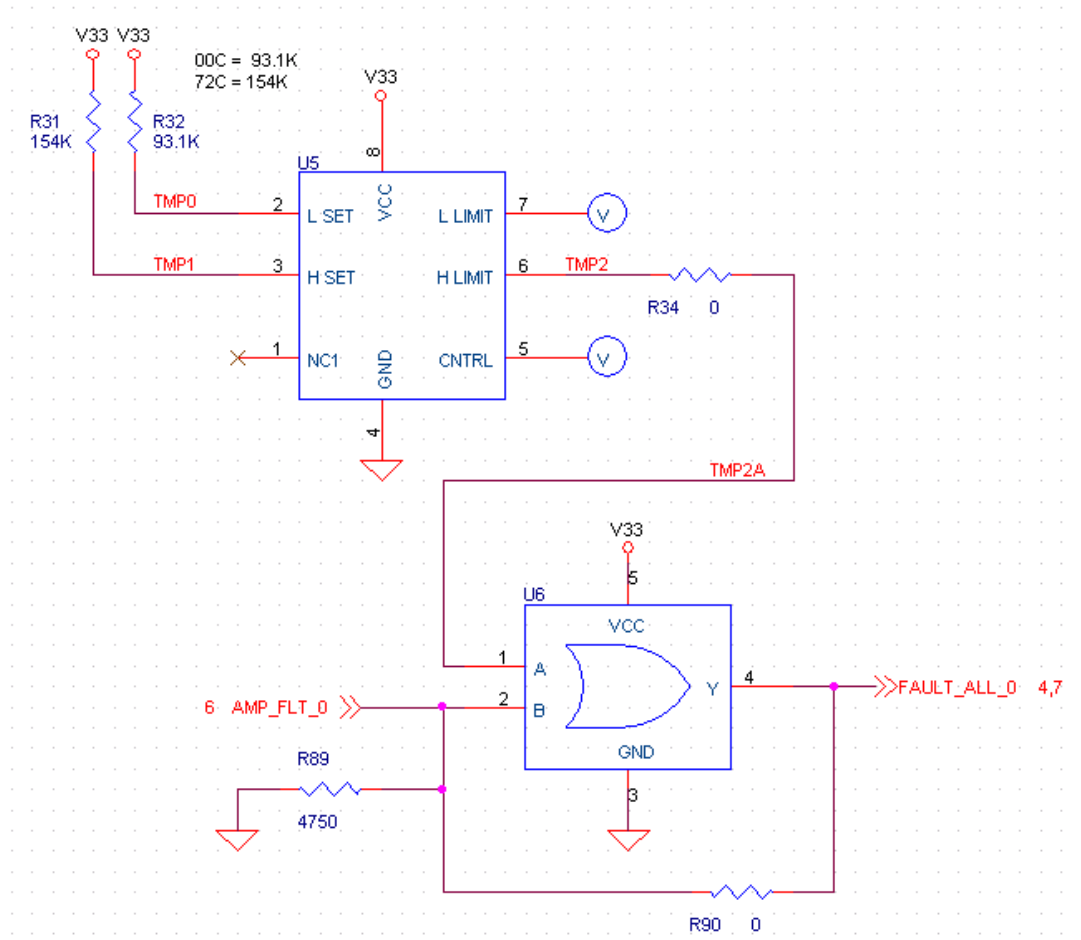


FIGURE 5 – MT FAULT GENERATION

Relay Over-Temperature (RT) fault can be generated by either axis 0 or axis 1 of the RMB, and the fault is specific to the AMP FAULT of the axis that generated it. The fault is generated by the diagnostic output of the solid state relays (SSR) used to provide 2 high-current outputs for each axis of the RMB. One SSR output pin is used to drive the external BRAKE control pin (J6 pin 8) and a second SSR output pin is used to drive the USER OUT control pin (J4 pin 4). The SSR package provides a diagnostic output to indicate an over temperature condition of either the BRAKE or the USER OUT driver. See Figure 6. The active state of the diagnostic output is AND'd into the axis AMP FAULT chain. If either the BRAKE output or the USER OUT output is faulted due to excessive current (over temperature) an amplifier fault will be generated.

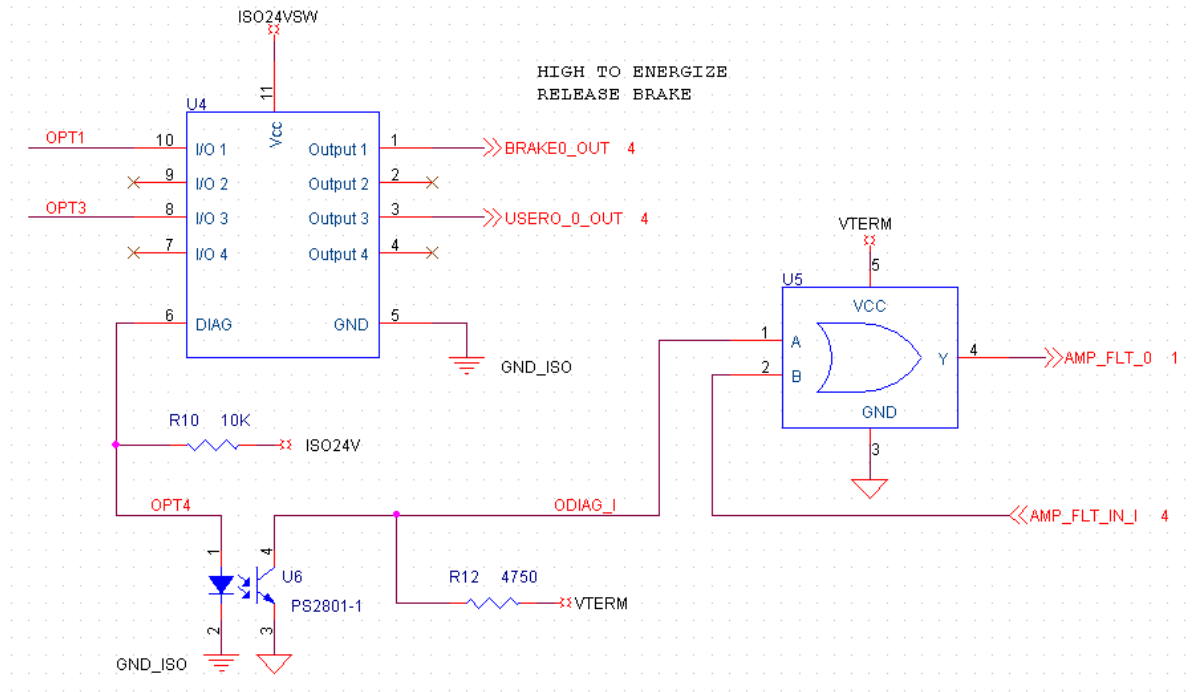


FIGURE 6 – RT FAULT GENERATION

The FPGA does not differentiate between AMP FAULT, MT, and RT conditions. It does differentiate between axis 0 and axis 1 faults. One method to apply in determining the source of a single fault is as follows:

- The FAULT LED's for axis 0 and axis 1 will determine which axis is causing the fault.
- If the FAULT LED is lit for either axis 0 or axis 1, remove the J5 cable connection from that axis. If the FAULT LED goes out, the fault is being caused by the J5 connection to the amplifier.
- If the FAULT LED remains lit, disconnect the J6 MOTOR connector. If the FAULT LED goes out, the fault is being caused by the BRAKE output driver being over-temperature.
- If the FAULT LED remains lit, disconnect the J4 SENSOR connector. If the LED goes out, the fault is being generated by the USER OUT output driver being over-temperature.
- If the FAULT LED remains lit, the only remaining source is the MT source inside the module. Remove power from the module, let it cool, then apply power and see if the fault condition remains or returns.

4.6 SHUTDOWN INPUT

The RMB implements a method for the user to initiate a node disable from an external source. This can be done through a hardware input present on both axis 0 and axis 1.

Axis 0 and 1 each provide a pair of input pins on the axis SENSOR connector J6. These pins are SHUTDOWN+ (J6 pin 17) and SHUTDOWN- (J6 pin 18). Assertion (positive bias) of the SHUTDOWN input pin pair with 24Vdc at 5mA (min) will disable the node. The SHUTDOWN+ pin and the SHUTDOWN- pin are connected to the anode and cathode legs (respectively) of an OPTO-isolator, limited internally with a 5.11K resistor. The user can elect to bias the OPTO input circuit as a high-side switch or a low-side switch. Bias must be applied externally, using J6 pin 26 (ISO24V), one of the isolated ground return pins, and the user switch or control.

- If the input is disconnected or not biased, SHUTDOWN is not asserted. Note that this is the default state with no user connection.
- If the input is biased on, SHUTDOWN is asserted. This means disable the node.

The SHUTDOWN circuits on axis 0 and axis 1 are identical, the description and Figure 7 apply equally to both axes. (Note that early revision RMB modules used a single-ended input model for axis 0. For additional information see Appendix B).

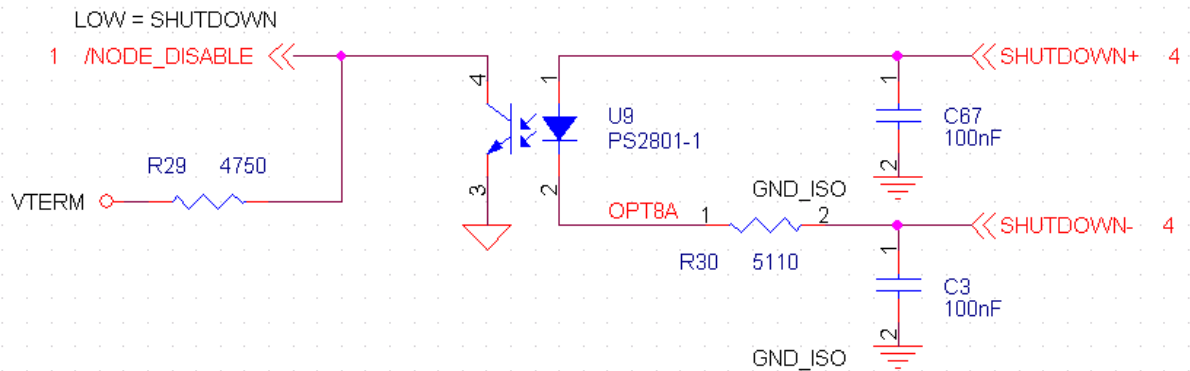


FIGURE 7 – SHUTDOWN INPUT CIRCUIT

4.7 ANALOG OUTPUTS

The analog output circuits on the RMB are designed to allow the user to drive a -10Vdc to +10Vdc output voltage in a bipolar fashion. Serial DAC's are used in cascade, with the CMD DAC first in the chain and the AUX DAC second. All DAC's are controller directly by the SynqNet FPGA and are time-synchronized. Axis 0 and axis 1 output circuits are the same. Axis 0 is detailed in Figure 8.

Each DAC output is connected to the J5 connector via an analog switch. The analog switch is controlled by a reset monitor connected to VTERM (3.3V). This monitor is used to assure that the DAC outputs are disconnected from all external circuits during power supply startup and stabilization.

Each DAC output block presents two output pins to the user on J5. Each pair of J5 connector analog output pins is routed from the right side of Figure 8, examples shown are nets CMD_DAC_OUT_0 (+/-) and AUX_DAC_OUT_0 (+/-). The front panel connector (-) pins for all DAC's are internally connected to analog ground.

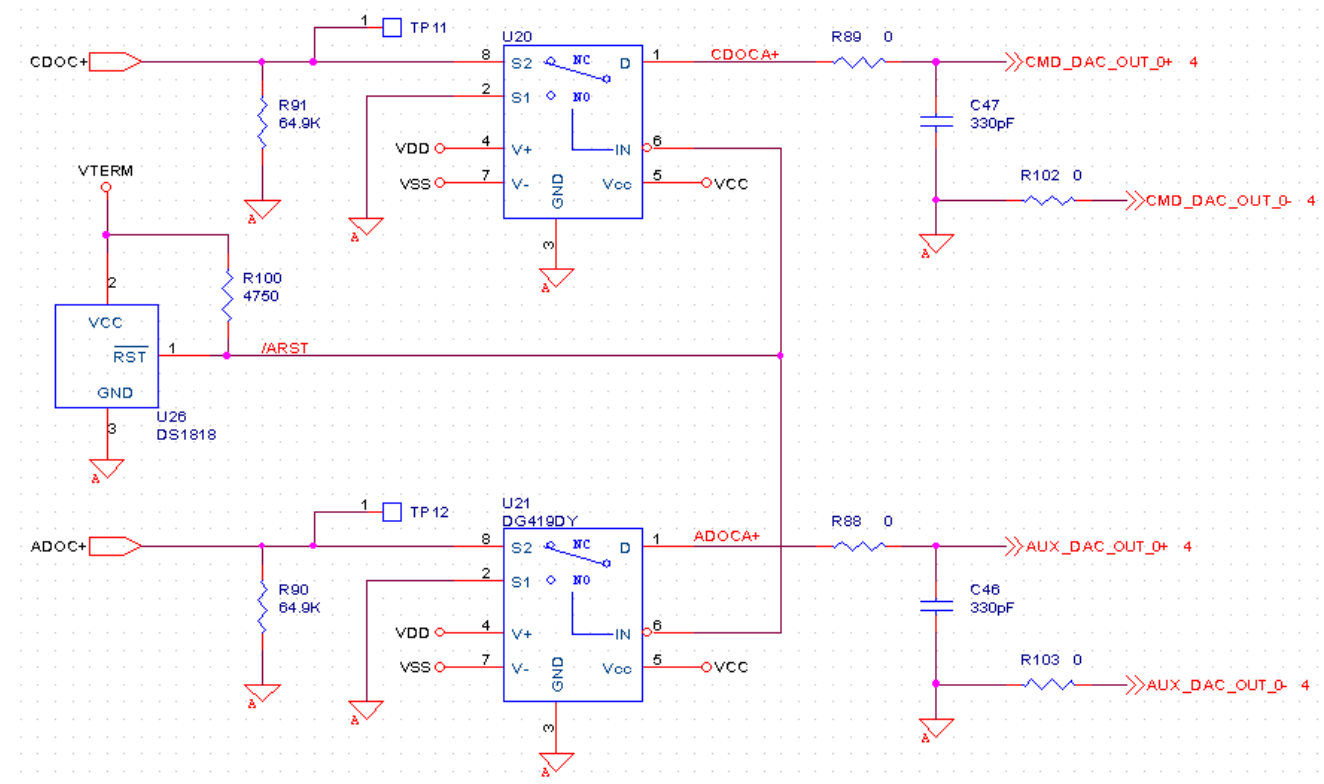


FIGURE 8 – ANALOG OUTPUT DAC CIRCUITS

4.8 ENCODER INPUTS

The RMB implements quadrature encoder inputs for each axis. The axis 0 and axis 1 input circuits are identical. Axis 0 is detailed in Figure 9.

Encoder inputs originate on connectors J6-0 and J6-1. Each quadrature input A and B, and index input Z are true differential inputs. Single-ended operation is not supported. Each input pin pair is terminated internal to the RMB module with a 274 ohm resistor. Fail-safe terminations are NOT provided, as this would defeat the quadrature decoder broken-wire sensing. The quadrature decoder presents the decoded pulse train and index to the FPGA. It also generates a broken-wire alarm signal that is asserted when an input is detected within an invalid level or at an invalid state.

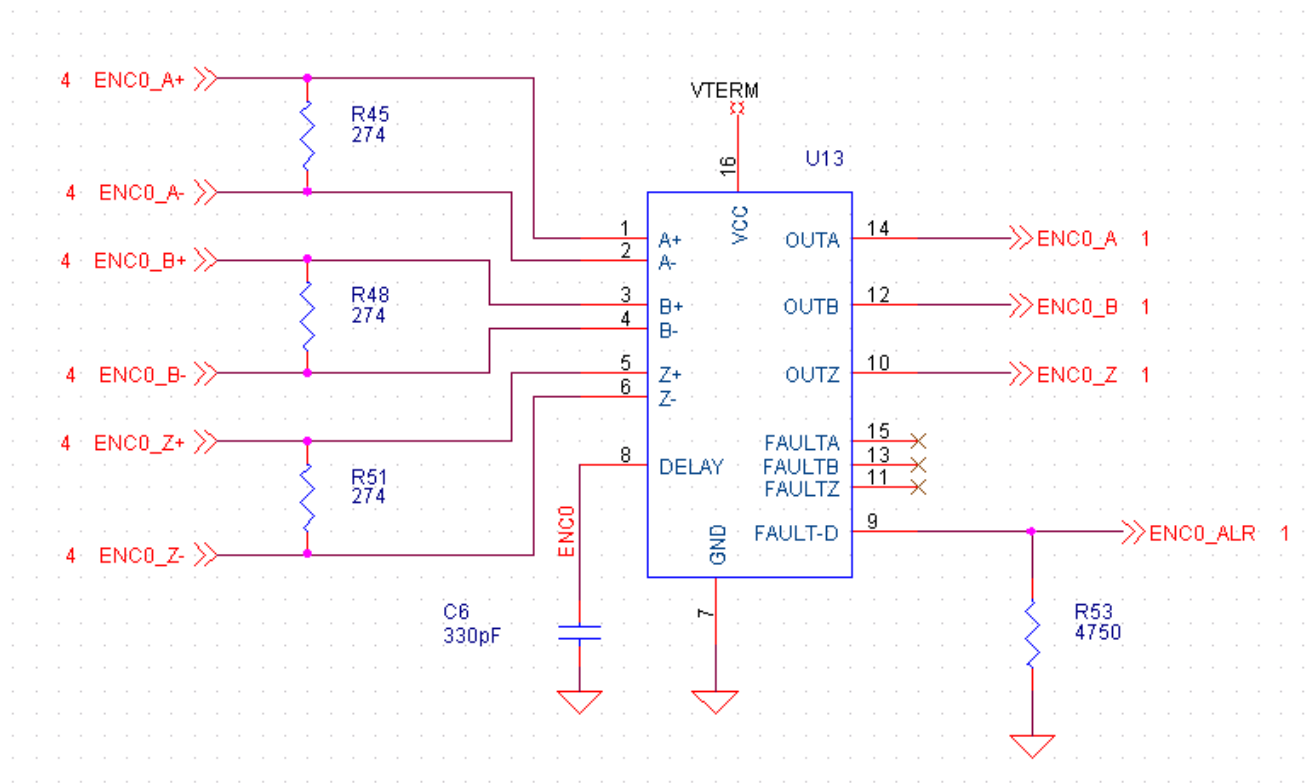


FIGURE 9 – ENCODER INPUT CIRCUIT

4.9 HALL SENSOR INPUTS

The RMB implements HALL sensor inputs for each axis. The axis 0 and axis 1 input circuits are identical. Axis 0 is detailed in Figure 10.

Hall inputs are located on connectors J6-0 (axis 0) and J6-1 (axis 1). The inputs are optically isolated, with the capability of being either a differential 5V active-off input or a single-ended 5V active-high input. Note that HALL active levels can be switched within the FPGA under SW control. When used as a differential input, the HALL+ pin and the HALL- pin should be driven by a 26LS31 driver (or equivalent). When used as a single-ended input, the HALL+ pin should remain unconnected. The HALL- pin should be driven by a TTL open-collector drive (or equivalent).

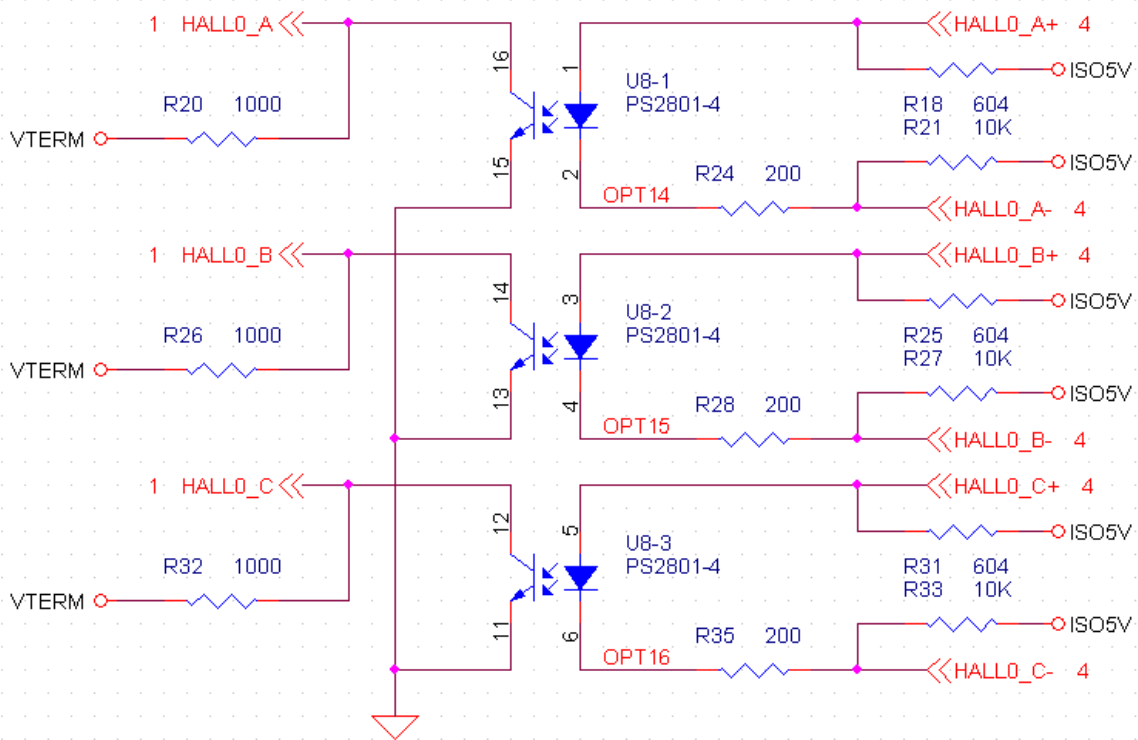


FIGURE 10 – HALL A, B, AND C INPUT CIRCUITS

4.10 LIMIT SENSOR INPUTS

The RMB implements a HOME, POSITIVE LIMIT, and NEGATIVE LIMIT sensor input for each axis. The axis 0 and axis 1 circuits are identical. Axis 0 is detailed in Figure 11.

Input circuits consist of an optical isolator input connected to internal ISO24V, and a 5.11K current limiting resistor connected to the J4 SENSOR connector pin 6. This input asserts active if disconnected, thus all limit inputs will be asserted if a cable is disconnected. All inputs require an active-low external switch, capable of 5mA.

The input circuits are shown, with the limits being true if the cable is disconnected, with the external switch pole being closed when in travel (limit false) and open outside the limit (limit true).

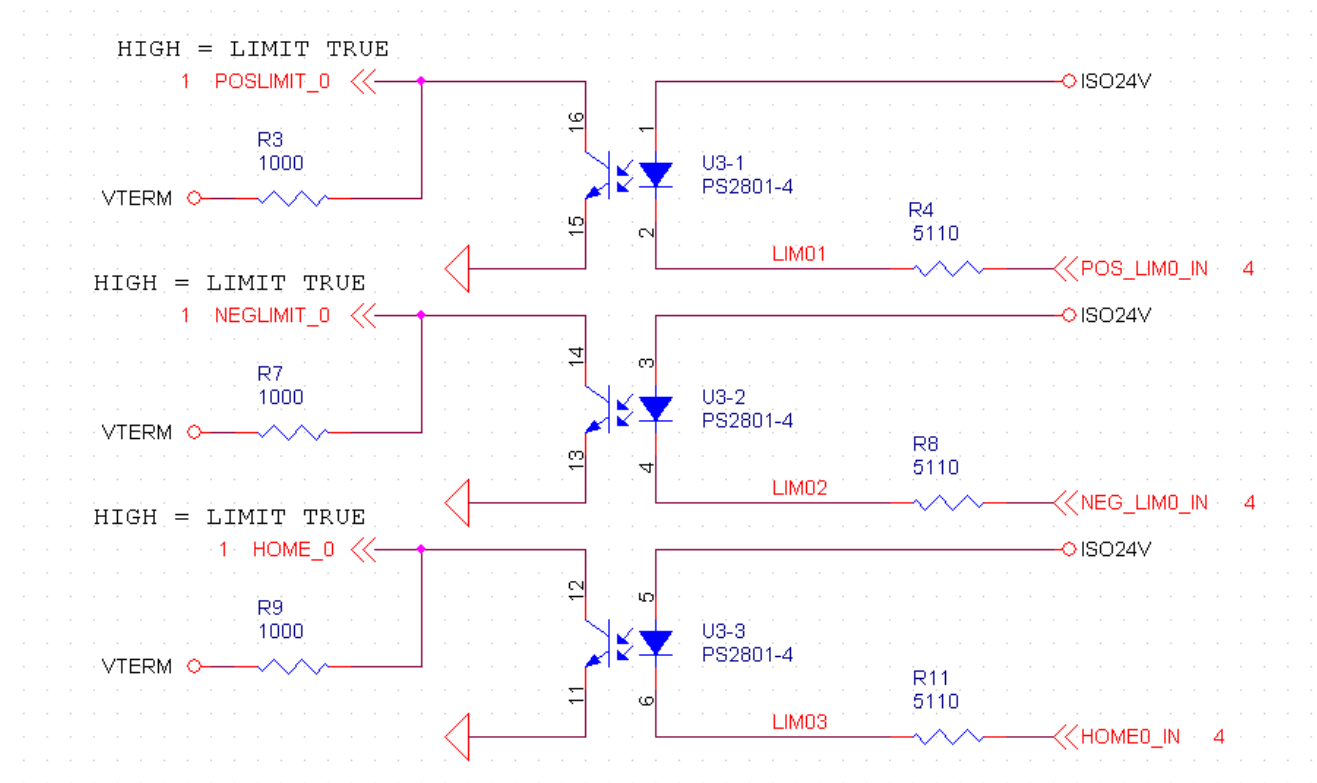


FIGURE 11 – HOME, PLIM, AND NLIM INPUT CIRCUITS

4.11 CAPTURE INPUT

The RMB implements a capture input for each axis. The axis 0 and axis 1 input circuits are identical. Axis 0 is detailed in Figure 12.

Input circuits consist of an optical isolator anode and cathode connected to the J4 SENSOR connector, with a 5.11K ohm current limiting resistor in the cathode leg of the circuit. This input asserts an active input when unbiased, thus the capture input will be held asserted if a cable is disconnected. The source and return bias pins for connection of an external user switch are available on J4.

The input circuit is shown in Figure 13. An external series switch pole capable of 24Vdc @ 5mA would be closed to de-assert the input, and open to assert the input. The capture input will be asserted if the cable is disconnected.

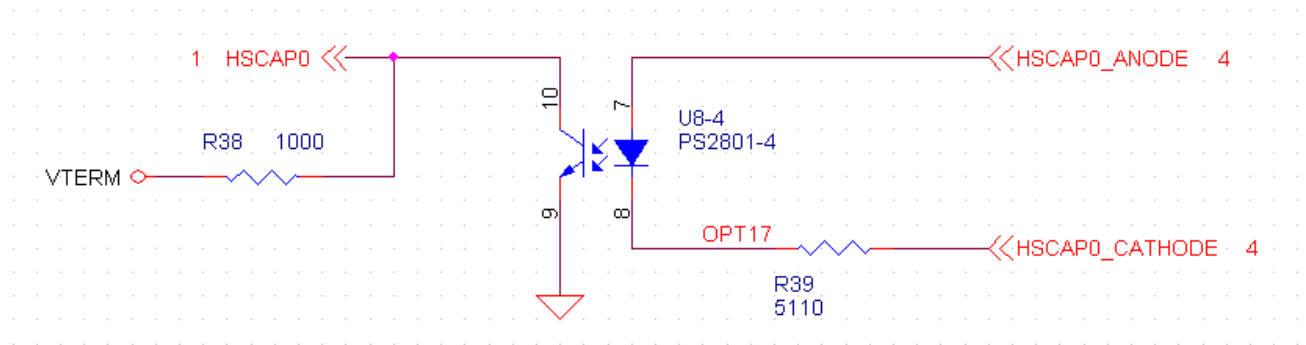


FIGURE 12 – CAPTURE INPUT CIRCUIT

4.12 USER INPUT

The RMB implements a USER input for each axis. The axis 0 and axis 1 input circuits are identical. Axis 0 is detailed in Figure 13.

Input circuits consist of an optical isolator input connected to internal ISO24V, and a 5.11K current limiting resistor connected to the J4 SENSOR connector pin 14. An external series switch pole capable of 24Vdc @ 5mA would be closed to de-assert the input, and open to assert the input. The USER IN input will be asserted if the cable is disconnected.

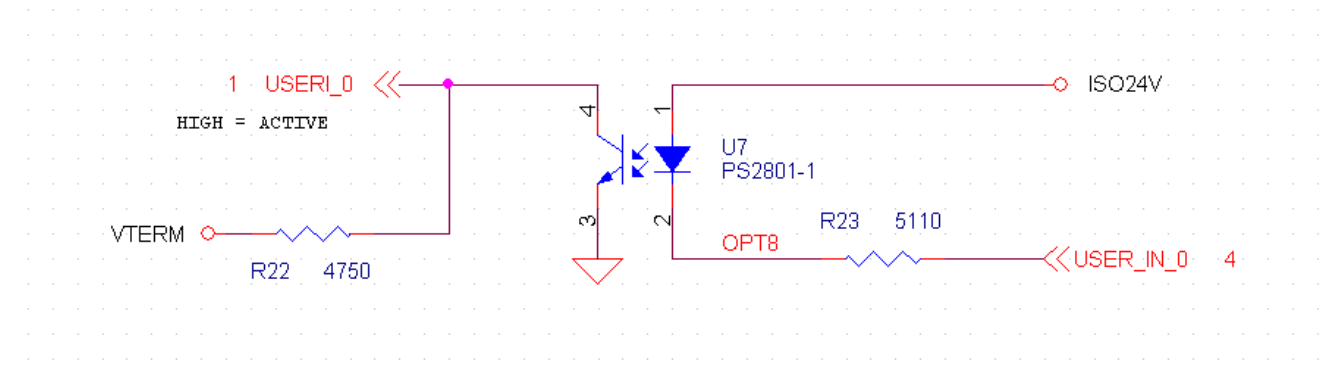


FIGURE 13 – USER IN CIRCUITS

4.13 USER OUTPUT

The RMB implements a USER output for each axis. The axis 0 and axis 1 output circuits are identical.

The USER OUT function on connectors J4-0 and J4-1 each consist of the control pin (J4 pin 4), and a dedicated return pin (J4 pin 9). The USER OUT driver circuit is both optically isolated and buffered using a high-current solid state relay (SSR) as a high-side switch. The output will be 1.5Vdc (maximum) when the SSR driver is off. The output will be a low impedance path to internal isolated 24V (0.4 ohm maximum) when the SSR driver is on. The output states are controlled by hardware and FPGA logic as follows:

Hardware State	USER OUT Relay State
During Power On	Off
During Hardware Reset	
During FPGA Configuration	
After FPGA Configuration	
USER OUT Asserted	On

This circuit is designed to an additional high-current control output for user assignment. Each SSR driver is rated for 500ma (maximum), and is thermally protected from over-current conditions. A SSR driver will disconnect and generate an AMP fault signal (specific to the axis of control) if it overheats. Other drivers are not affected. When the overheated SSR driver cools it will reconnect and the AMP fault signal will be removed. This cycle will continue until the source of the thermal fault is removed.

4.14 LED STATUS INDICATORS

The RMB module contains 22 LED's which are all located on the front panel. Status LED's are assigned to SynqNet interface and axis interface functions as follows:

- D1 through D6 are status LED's for the SynqNet interface
- D7 through D14 are status LED's for Axis 0
- D15 through D22 are status LED's for Axis 1

These indicators are displayed pictorially in Figure 14 at the end of this section. The function of SynqNet status LED's D1 through D6 is as follows:

LED	Name	Color	Meaning when on	Controlled by	Modes
D1	STATUS	Blue	FPGA boot successful	FPGA	Off/Blink/On
D2	NODE	Green	Node state	FPGA	Off/Blink/On
D3	REPEAT	Green	Repeater ON	FPGA	Off/Blink/On
D4	IN ACT	Green	Link active	PHY	Off/On
D5	OUT ACT	Green	Link active	PHY	Off/On
D6	ALARM	Red	Node alarm exists	FPGA	Off/On

D1, D2, D3, and D6 are used to indicate normal node operating status as follows:

Node state	STATUS Blue (D1)	NODE Green (D2)	REPEAT Green (D3)	ALARM Red (D6)
Unpowered	OFF	OFF	OFF	OFF
HW Reset	OFF	OFF	OFF	OFF
Undiscovered	BLINK .37 Hz	BLINK (1)	OFF	ON
Discovered	BLINK .75 Hz	BLINK (1)	OFF	ON
SYNQ	ON	ON	ON or OFF (3)	OFF
SYNQ lost	BLINK 1.5 Hz	BLINK (2)	BLINK (4)	ON

- (1) Blinks in same phase as **STATUS**
- (2) Blinks in opposite phase of **STATUS**
- (3) On if not node N-1, otherwise off
- (4) Off if node 0, otherwise blink in same phase as **STATUS**

For **STRING** networks, if all nodes are in SYNC, the normal state of nodes 0 through node n-1 is to have **STATUS**, **NODE**, **REPEAT**, **IN ACT**, and **OUT ACT** continuously on. Node N (the last node) will have **STATUS**, **NODE**, and **IN ACT** continuously on.

For **RING** networks, if all nodes are in SYNC, the normal state of nodes 0 through node n-1 is to have **STATUS**, **NODE**, **REPEAT**, **IN ACT**, and **OUT ACT** continuously on. Node N (the last node) will have **STATUS**, **NODE**, **IN ACT**, and **OUT ACT** continuously on.

The function of Axis 0 status LED's D7 through D14 are as follows:

LED	Name	Color	Meaning when on
D7	BRAKE	Red	Brake is on (unbiased)
D8	HOME	Green	Home input is activated
D9	POS LIM	Red	Positive limit input is active
D10	NEG LIM	Red	Negative limit input is active
D11	ENABLE	Green	Enable output is active
D12	FAULT	Red	Amp fault input is active
D13	USER OUT	Green	User output is active
D14	USER IN	Green	User input is active

The function of Axis 1 status LED's D15 through D22 are as follows:

LED	Name	Color	Meaning when on
D15	BRAKE	Red	Brake is on (unbiased)
D16	HOME	Green	Home input is activated
D17	POS LIM	Red	Positive limit input is active
D18	NEG LIM	Red	Negative limit input is active
D19	ENABLE	Green	Enable output is active
D20	FAULT	Red	Amp fault input is active
D21	USER OUT	Green	User output is active
D22	USER IN	Green	User input is active

Note that although present, LED's D15 through D22 are held in the off state on the TA801 products.

RMB		
STATUS	BLUE	D1
NODE	GREEN	D2
REPEAT	GREEN	D3
IN ACT	GREEN	D4
OUT ACT	GREEN	D5
ALARM	RED	D6
AXIS 0		
BRAKE	RED	D7
HOME	GREEN	D8
POSLIMIT	RED	D9
NEGLIMIT	RED	D10
ENABLE	GREEN	D11
FAULT	RED	D12
USER OUT	GREEN	D13
USER IN	GREEN	D14
AXIS 1		
BRAKE	RED	D15
HOME	GREEN	D16
POSLIMIT	RED	D17
NEGLIMIT	RED	D18
ENABLE	GREEN	D19
FAULT	RED	D20
USEROUT	GREEN	D21
USER IN	GREEN	D22

FIGURE 14 – PANEL VIEW OF STATUS INDICATORS

4.15 DTS OUTPUTS

The RMB implements two DTS outputs for each axis. The axis 0 and axis 1 input circuits are identical. Axis 0 is detailed in Figure 15.

The DTS outputs can be used to select the transconductance ratio on specific Trust Automation amplifiers. Table 2 lists examples of DTS control on four Trust Automation amplifiers. These input bits function to control the amplifier transconductance as shown. (Note that on all amplifiers DTS signals must be connected between the RMB and the amplifier and amplifier DTS switches must be set into the UP position for remote DTS to function).

TA105/TA305 Transconductance Setting	DTS MSB (select Bit 1) J1 pin 6 S1 Position 6	DTS LSB (select Bit 0) J1 pin 5 S1 Position 5
10V in = 0.5A out	0	0
10V in = 1.0A out	0	1
10V in = 1.5A out	1	0
10V in = 2.0A out	1	1
TA115/TA310 Transconductance Setting	DTS MSB (select Bit 1) J1 pin 6 S1 Position 6	DTS LSB (select Bit 0) J1 pin 5 S1 Position 5
10V in = 2.0A out	0	0
10V in = 4.0A out	0	1
10V in = 6.0A out	1	0
10V in = 8.0A out	1	1
TA320 Transconductance Setting	DTS MSB (select Bit 1) P5 pin 12	DTS LSB (select Bit 0) P5 pin 11
10V in = 3.0A out	0	0
10V in = 6.0A out	0	1
10V in = 9.0A out	1	0
10V in = 12.0A out	1	1

Table 2 – DTS Pin Functions

The DTS output circuits are optically isolated outputs that are configured as a low-side switch connected internally to isolated ground. Each collector output has an internal pullup to isolated 5Vdc. When the FPGA asserts DTS, the output pin will be released and pulled high. When the FPGA de-asserts DTS, the output pin will be driven low.

The DTS output circuits can also be used as general-purpose output bits, if not dedicated to DTS functions.

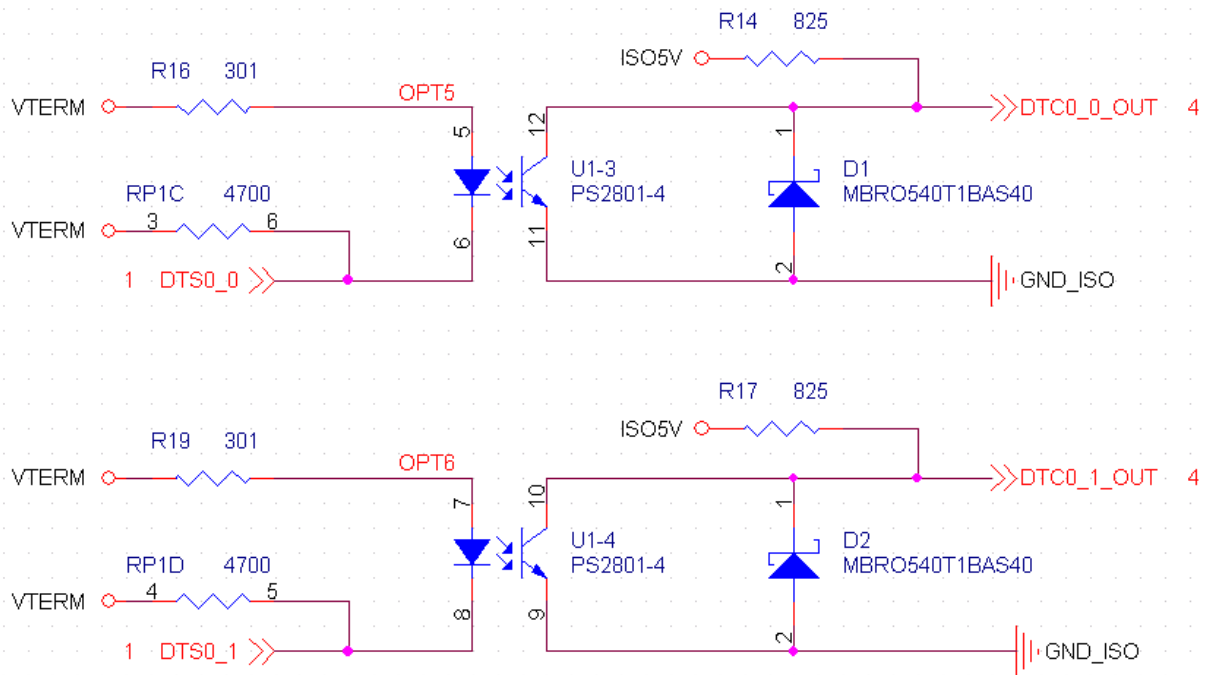


FIGURE 15 – DTS OUTPUT CIRCUITS

4.16 STEPPER TRANSCEIVER OUTPUTS

The RMB implements STEP and DIRECTION control outputs for each axis. These outputs allow for the control of one stepper motor per axis. The axis 0 and axis 1 output circuits are identical. Axis 0 is detailed in Figure 16.

The STEP and DIRECTION outputs on the RMB are RS-422 drivers that are 26LS31 equivalents. These drivers allow the use of single-ended or differential stepper motor inputs. Both USER RS-422 output circuits are identical to the STEP and DIRECTION outputs. For environments with high levels of electrical noise, differential connections are recommended. Note that internal terminations detailed in Figure 16 are NOT loaded on the factory default configuration. Standard termination practices for RS-422 interfaces detail that the cable terminations be loaded at the opposite end of the interface cable from the driver. For specific termination requirements, contact Trust Automation.

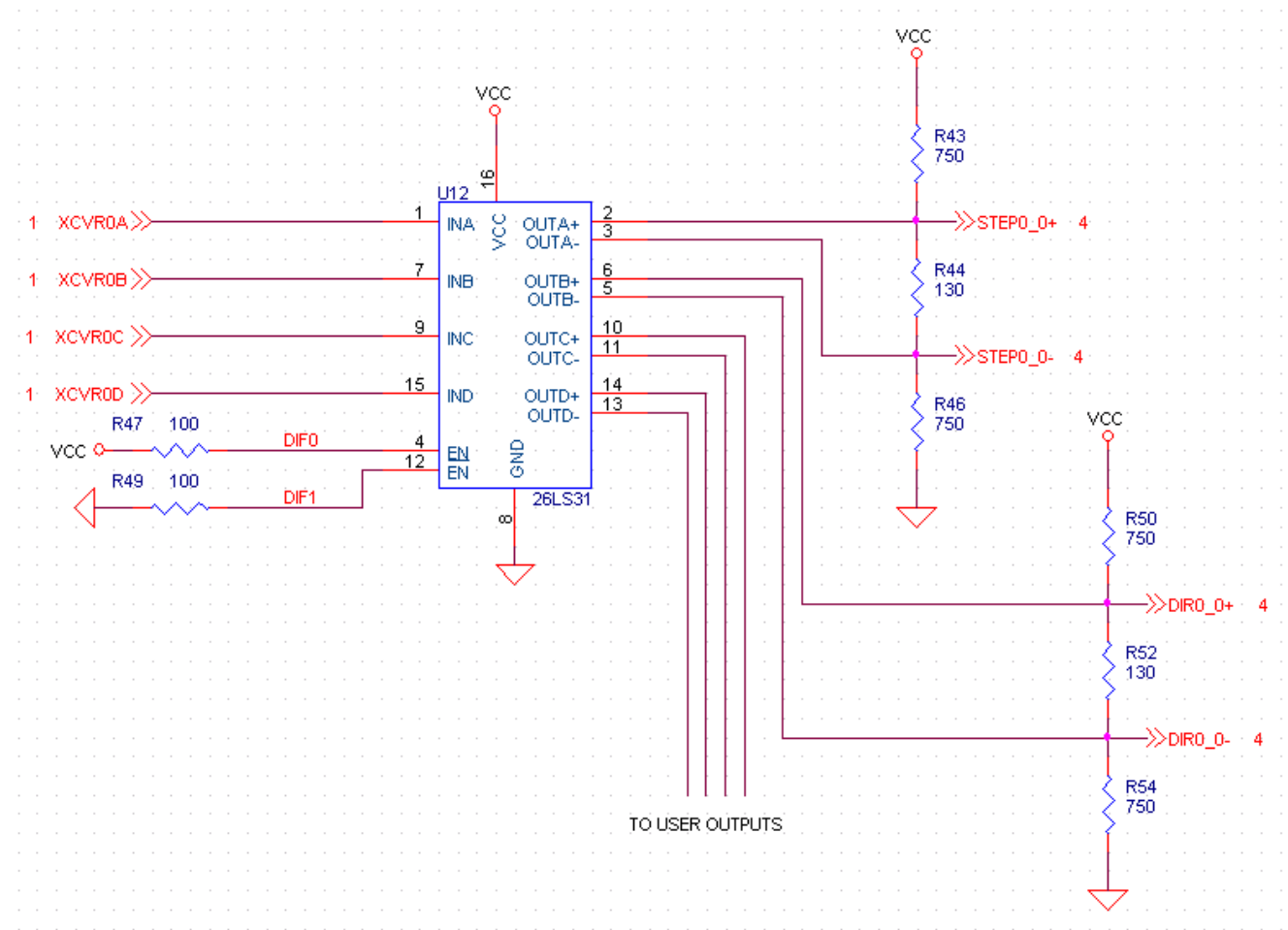


FIGURE 16 – STEP/DIR OUTPUT CIRCUITS

4.17 RMB POWER INLET

Figure 17 shows the circuit protection elements in the power inlet stage. This circuit block is provided for reference only. Note that a 3A PTC combination and blocking diode protect the J3 24V input path. The isolated 24V and isolated 5V supplies present on the frontplate connectors are each protected by a 1.5A PTC.

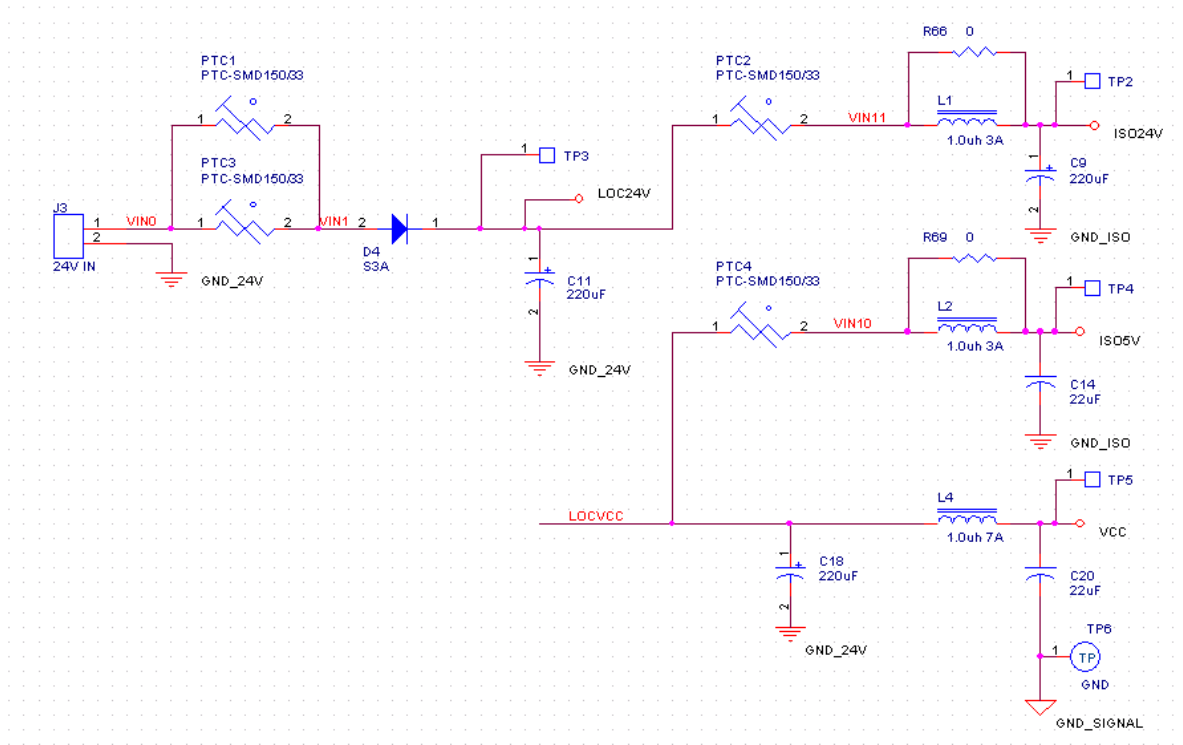


FIGURE 17 – POWER INLET CIRCUIT

5 CONNECTORS

The RMB contains several panel connectors for external connections. These are designated as follows:

- J1 – SynqNet Interface IN connector
- J2 – SynqNet Interface OUT connector
- J3 – 24VDC power inlet connector
- J4-0, J4-1 – SENSOR Connector
- J5-0, J5-1 – DRIVE Connector
- J6-0, J6-1 – MOTOR Connector

Each connector type and style is described in additional detail in the following sections.

5.1 SYNQNET INTERFACE IN CONNECTOR (J1)

The SynqNet IN J1 connector is located on the bottom angled edge of the RMB module. The connector is an RJ-45 style connector, is labeled as 'IN', and is the RJ-45 connector closest to the front (DB connectors) of the module. The board mounted connector is a Molex 85504-0001. Note that the Molex 85504 connector provides connectivity for shielded Ethernet cables. Shielded cables are recommended for the SynqNet interface but are not required. A representative mating shielded connector could be Molex 95043 Family or equivalent.

PIN	SIGNAL
1	TXD+
2	TXD-
3	RXD+
4	CT
5	CT
6	RXD-
7	CT
8	CT
SHIELD	*

* The cable shield is capacitively coupled to the chassis, or frame.

Table 3 – SynqNet IN Port Pin Functions

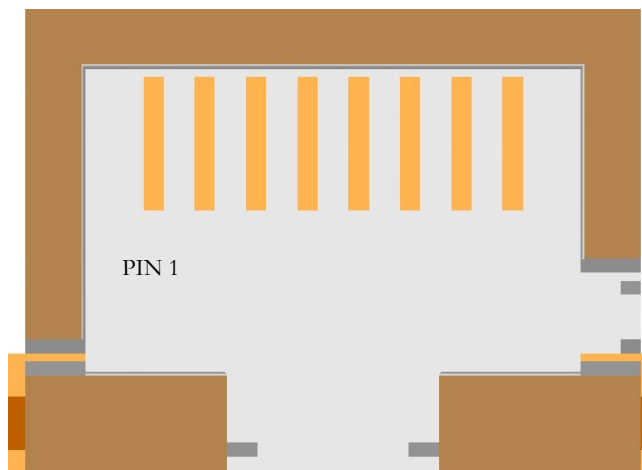


FIGURE 18 – J1 IN CONNECTOR FRONT VIEW

5.2 SYNQNET INTERFACE OUT CONNECTOR (J2)

The SynqNet OUT J2 connector is also located on the bottom angled edge of the RMB module. The connector is an RJ-45 style connector, is labeled as ‘OUT’, and is the RJ-45 connector closest to the rear (bulkhead flange) of the module. The board mounted connector is a Molex 85504-0001. Note that the Molex 85504 connector provides connectivity for shielded Ethernet cables. Shielded cables are recommended for the SynqNet interface but are not required. A representative mating shielded connector could be Molex 95043 Family or equivalent.

PIN	SIGNAL
1	RXD+
2	RXD-
3	TXD+
4	CT
5	CT
6	TXD-
7	CT
8	CT
SHIELD	*

* The cable shield is capacitively coupled to the chassis, or frame.

Table 4 – SynqNet OUT Port Pin Functions

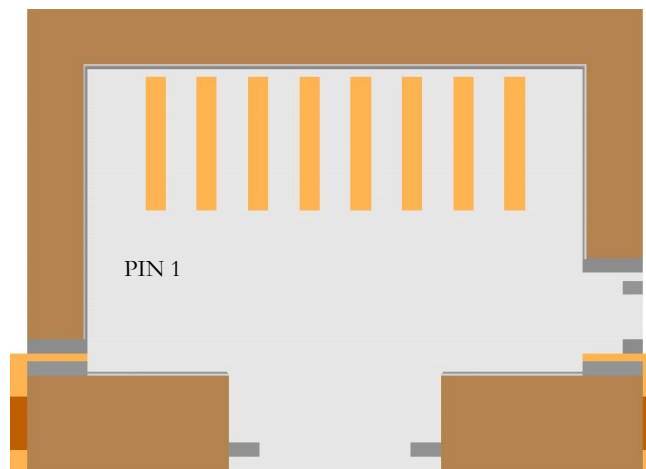


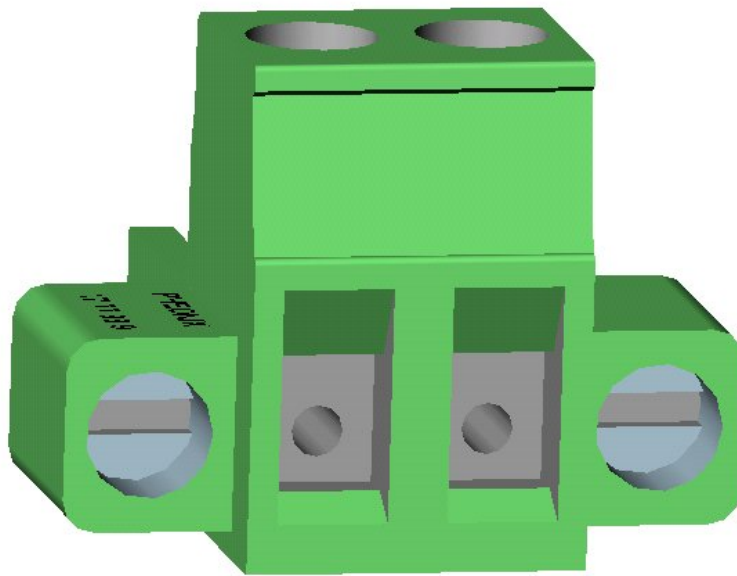
FIGURE 19 – J2 OUT CONNECTOR FRONT VIEW

5.3 POWER INLET CONNECTOR (J3)

The power inlet connector J3 is located on the bottom of the RMB SynqNet module. The board mounted connector is a Phoenix Contact Combicon™ family P/N 17 76 50 8. The external mating connector is a Phoenix Contact P/N 17 77 98 9 (TPN CON-0455-M1), and is supplied with every RMB module. Note that the Phoenix Contact connector accepts wires sizes between 12 and 24 AWG. The required RMB inlet voltage is 24VDC +/- 3VDC. The RMB inlet power path is protected with a 3A PTC and a 3A blocking diode.

The RMB provides isolated 24Vdc to the user via front panel connectors J4 (pins 1, 2, and 3). Note that these 24V source pins are isolated from the inlet supply with a 2.5A resettable circuit protection device (PTC) and a filter network.

Note: If the RMB input voltage is 24.0Vdc, the isolated 24VDC provided to the user on front panel connectors J4 and J5 will be between 23.2 and 23.4 Vdc. This is due to the voltage drop of the protection device and blocking diode.



Source	Return
Positive	Negative

FIGURE 20 – J3 MATING CONNECTOR FRONT VIEW

5.4 SENSOR CONNECTOR (J4-0 AND J4-1)

The J4 connector(s) are 15 pin female high density D-Sub style(s). The connector used in the RMB is a Kycon K66-B15S-N. Representative mating connectors are NORCOMP 180-015-102-001 (solder cup) and NORCOMP 180-015-172-000 (crimp). A representative backshell kit is NORCOMP 977-009-020-121.

The following Figure and Tables detail the pin assignments and definitions of J4:

RMB - J4-0 / J4-1					
SENSOR					
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	ISO24V	6	HOME	11	IRTN
2	ISO24V	7	LIM+	12	IRTN
3	ISO24V	8	LIM-	13	IRTN
4	USERO	9	IRTN	14	USERI
5	HSCAP+	10	HSCAP-	15	FRAME

Table 5 – J4 Pin Assignments

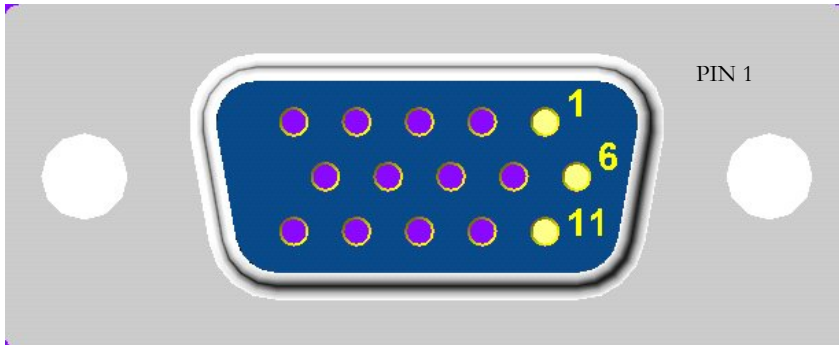


FIGURE 21 – J4 CONNECTOR FRONT VIEW

PIN	Definition
1	Isolated 24V Supply
2	Isolated 24V Supply
3	Isolated 24V Supply
4	User Output
5	High Speed Capture Anode (+)
6	Home Input
7	Positive Limit Input
8	Negative Limit Input
9	Isolated GND return
10	High Speed Capture Cathode (-)
11	Isolated GND return
12	Isolated GND return
13	Isolated GND return
14	User Input
15	FRAME/Chassis Connection

Table 6 – J4 Pin Definitions

5.5 DRIVE CONNECTOR (J5-0 AND J5-1)

The J5 connector(s) are 15 pin male high density D-Sub style(s). The connector used in the RMB is a Kycon K66-B15P-N. A representative mating connector is NORCOMP 180-015-202-001 (solder cup) or NORCOMP 180-015-272-000 (crimp). A representative backshell kit is NORCOMP 977-009-020-121.

The following Figure and Tables detail the pin assignments and definitions of J5:

RMB - J5-0 / J5-1					
DRIVE					
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	CMD+	6	IOS5V	11	AUX+
2	CMD-	7	IRTN	12	AUX-
3	FAULT	8	ENABLE-	13	DTS0
4	STEP+	9	DIR+	14	DTS1
5	STEP-	10	DIR-	15	ENABLE+

Table 7 – J5 Pin Assignments

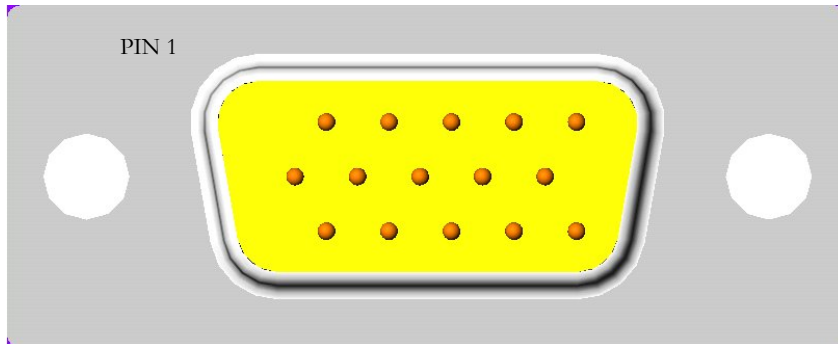


FIGURE 22 – J5 CONNECTOR FRONT VIEW

PIN	Definition
1	CMD DAC Output ($\pm 10\text{Vdc}$)
2	CMD DAC Return
3	Amplifier FAULT input (active high 5V input)
4	STEP 0 Positive Differential Output
5	STEP 0 Negative Differential Output
6	Isolated 5V Supply
7	Isolated GND return
8	Amplifier Output Enable Emitter (-)
9	DIR 0 Positive Differential Output
10	DIR 0 Negative Differential Output
11	AUX DAC Output ($\pm 10\text{Vdc}$)
12	AUX DAC Return
13	DTS 0 Output (5V OPTO)
14	DTS 1 Output (5V OPTO)
15	Amplifier Output Enable Collector (-)

Table 8 – J5 Pin Definitions

5.6 MOTOR CONNECTOR (J6-0 AND J6-1)

The J6 connector(s) are 26 pin female high density D-Sub style(s). The connector used in the RMB is a Kycon K66-B26S-N. A representative mating connector is NORCOMP 180-026-102-001 (solder cup) or NORCOMP 180-026-172-000 (crimp and poke). A representative backshell kit is NORCOMP 977-015-020-121.

The following Figure and Tables detail the pin assignments and definitions of J6:

RMB - J6-0 / J6-1					
MOTOR					
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	ENCA+	10	ENCB+	19	ENCZ+
2	ENCA-	11	ENCB-	20	ENCZ-
3	IRTN	12	IOS5V	21	IRTN
4	HALLA+	13	HALLB+	22	HALLC+
5	HALLA-	14	HALLB-	23	HALLC-
6	IRTN	15	IOS5V	24	IRTN
7	USERI	16	IRTN	25	FRAME
8	BRAKE	17	SDN+	26	ISO24V
9	IRTN	18	SDN-		

Table 10 – J6 Pin Assignments

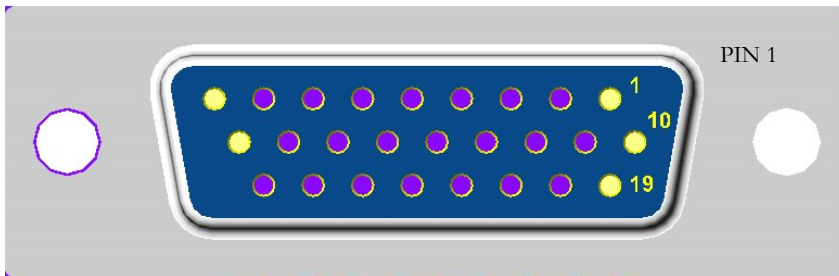


FIGURE 23 – J6 CONNECTOR FRONT VIEW

PIN	Definition
1	Encoder Quad A positive differential input (5V RS-422)
2	Encoder Quad A negative differential input (5V RS-422)
3	Isolated GND return
4	Hall A positive differential input (5V)
5	Hall A negative differential input (5V active low SE input)
6	Isolated GND return
7	USER input (24V active high)
8	Brake disable output (24V active high)
9	Isolated GND return
10	Encoder Quad B positive differential input (5V RS-422)
11	Encoder Quad B negative differential input (5V RS-422)
12	Isolated 5V Supply
13	Hall B positive differential input (5V)
14	Hall B negative differential input (5V active low SE input)
15	Isolated 5V Supply
16	Isolated GND return
17	SHUTDOWN Anode (24V bias to assert shutdown)
18	SHUTDOWN Cathode (24V bias to assert shutdown)
19	Encoder Index Z positive differential input (5V RS-422)
20	Encoder Index Z negative differential input (5V RS-422)
21	Isolated GND return
22	Hall C positive differential input (5V)
23	Hall C negative differential input (5V active low SE input)
24	Isolated GND return
25	FRAME/Chassis Connection
26	Isolated 24V Supply

Table 11 – J6 Pin Definitions

6 SPECIFICATIONS

This section lists the mechanical, electrical, and environmental specifications for the TA801 and TA802 RMB module family.

6.1 MECHANICAL DIMENSIONS – TA801

This section details the basic mechanical dimensions of the TA801 RMB modules. Overall size and mounting locations are provided.

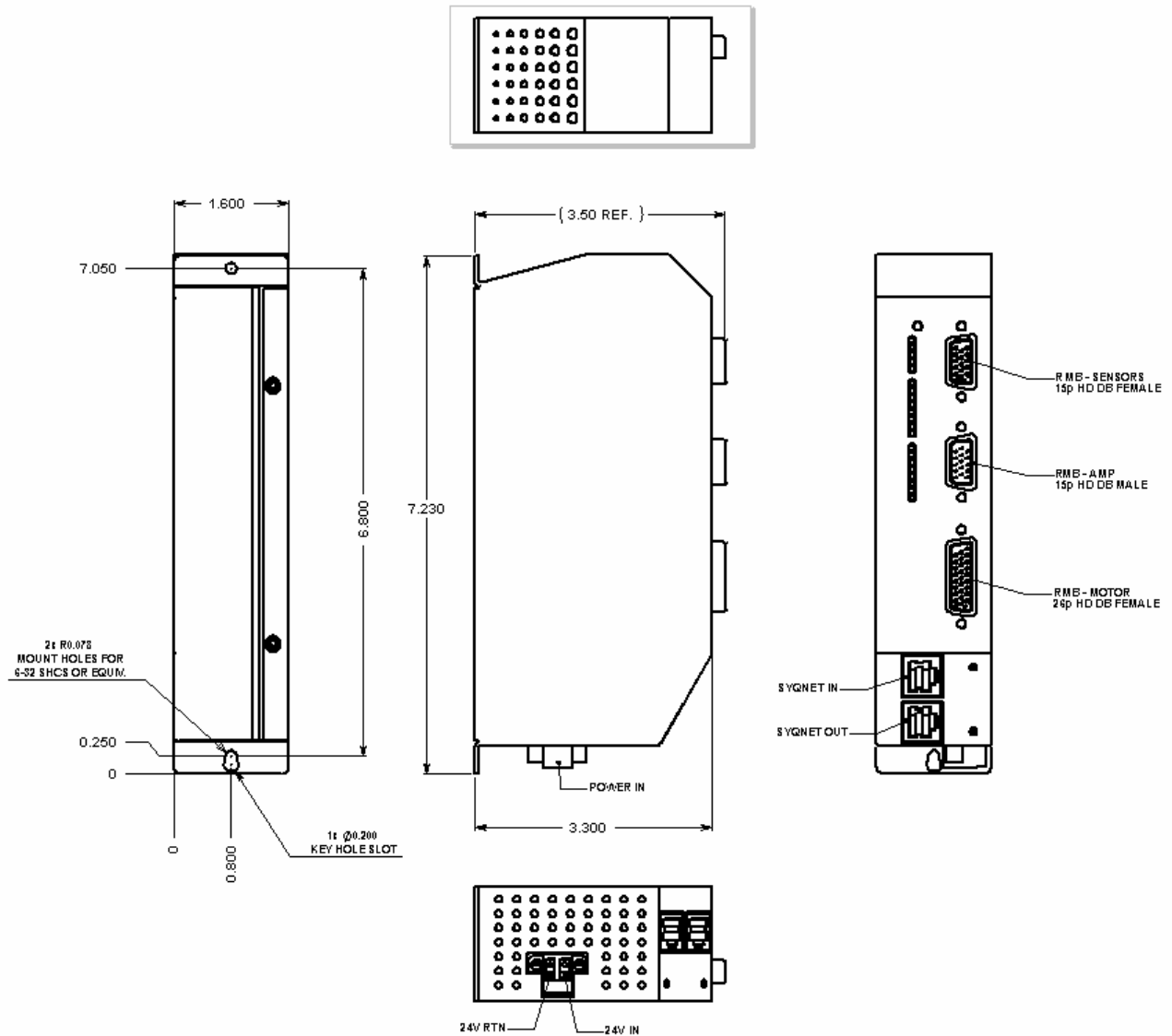


FIGURE 24 – TA801 MECHANICAL DIMENSIONS

6.2 MECHANICAL DIMENSIONS – TA802

This section details the basic mechanical dimensions of the TA802 RMB modules. Overall size and mounting locations are provided.

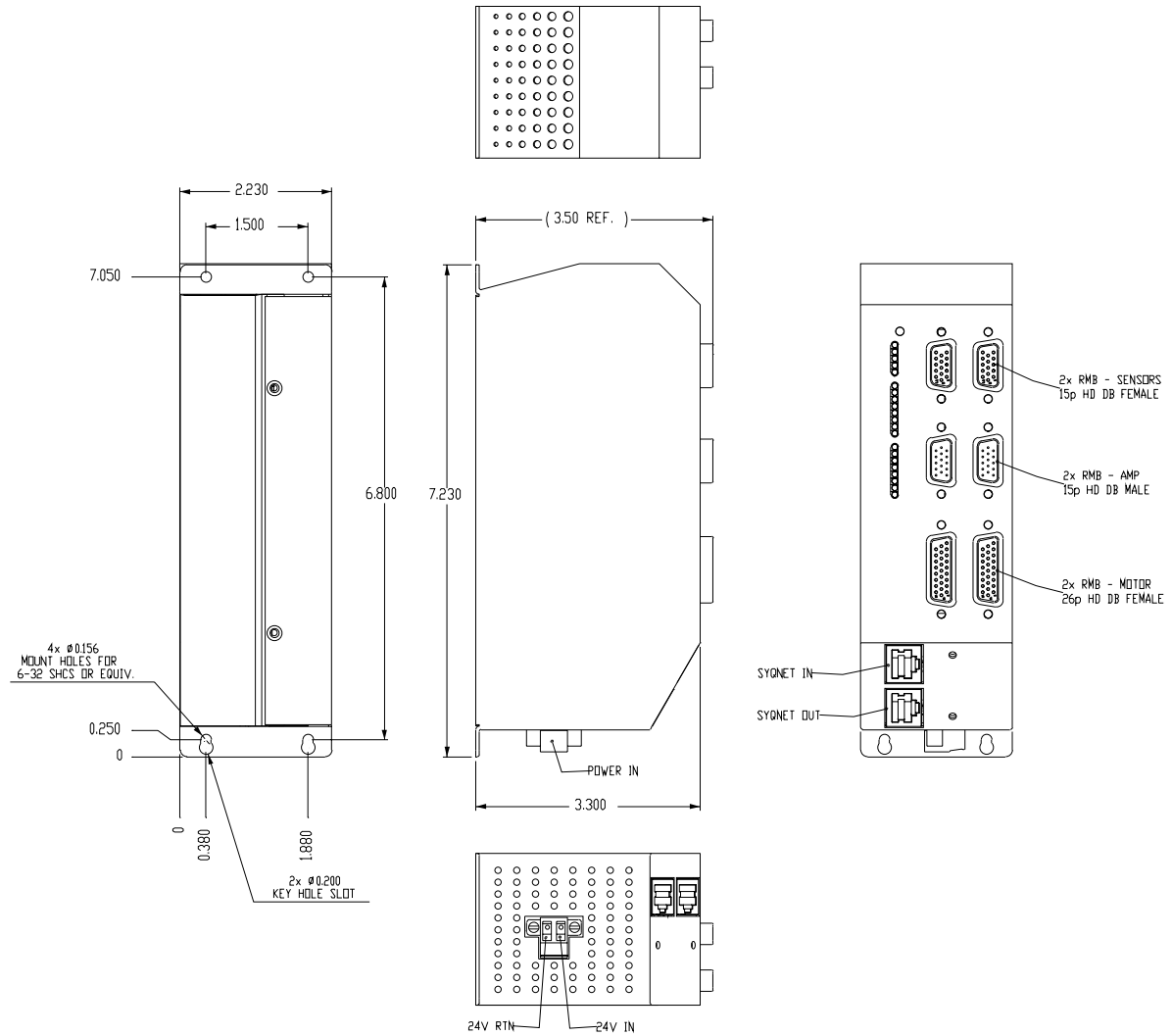


FIGURE 25 – TA802 MECHANICAL DIMENSIONS

6.3 ELECTRICAL

INPUT POWER REQUIREMENTS

The RMB requires the following input power based on internal and external power usage. Internal usage is consumed within the module by internal circuitry, external usage is dissipated external to the module via user components connected to the various power sources and return pins on J4, J5, and J6. Input voltage, current, and power requirements for the TA801 and TA802 RMB modules with no external usage are:

- Input Voltage: 24V +/- 3.0VDC, ripple/noise less than 300mVDC peak
- Input Current
 - TA801: 220 mA typical, 320 mA maximum
 - TA802: 270 mA typical, 370 mA maximum
- Internal Power
 - TA801: 5.3W typical, 7.7W maximum
 - TA802: 6.5W typical, 8.9W maximum

USER POWER CAPABILITIES

User (external) power usage is not considered part of the thermal cooling requirements for the module, but the user must account for external power usage in the system power budget.

- External 5V TA801 and TA802: 1.5A maximum, 7.5W maximum
- External 24V TA801 and TA802: 1.5A maximum, 36W maximum

The RMB can provide 5VDC power for external devices via the J5 and J6 front panel connectors. Available on J5 pin 6 and J6 pin 12. These power pins are all connected in common and protected by a 1.5A resettable circuit protection device (PTC).

The RMB can provide 24VDC power for external devices via the J4 and J6 front panel connectors. Available on J6 pin 26 and on J4 pins 1, 2, and 3. These power pins are all connected in common and protected by a 1.5A resettable circuit protection device (PTC).

ETHERNET

Ethernet Input/Output IEEE 802.3 100Base-TX (physical layer only)
 100Base-T CAT 5 or better cabling required
 Shielded cables recommended but not required
 100m length per link (max)

SIGNAL REQUIREMENTS

Shutdown Inputs: ON = 24Vdc @ 5 mA minimum
 OFF = no bias

Amp Fault Inputs: ON = no bias
 OFF = 1.0Vdc @ 5mA minimum

Encoder Inputs: Differential: 4.0Vdc @ 15mA RS-422 (A, B, Z)

Hall Inputs: Differential: ON = +4.0Vdc @ 15mA (A, B, C)
 OFF = Reverse Bias

Single-ended: ON = 0.5Vdc @ 5mA (A, B, C)
 OFF = no sink

HOME Inputs:	ON = no sink OFF = 1.0Vdc @ 5mA
PLIM, NLIM Inputs:	ON = no sink OFF = Sink 1.0Vdc @ 5mA
USER Inputs:	ON = No bias OFF = 0.5Vdc @ 2mA
Capture Inputs:	ON = Differential 24Vdc @ 5mA OFF = no bias Document rising edge and falling edge delays here...
Amp Enable Outputs:	ON = 5Vdc OPTO stage
Motor Brake Outputs:	ON = 24.0Vdc @ 500mA maximum OFF = no bias
DTS Outputs:	LOW = 0.5Vdc @ Ic = 2mA HIGH = 825 ohm pullup to 5Vdc
Command DAC Outputs:	+10.0Vdc to -10.0 Vdc, 10mA maximum
Auxiliary DAC Outputs:	+10.0Vdc to -10.0 Vdc, 10mA maximum
USER Outputs:	ON = 24.0Vdc @ 500mA maximum OFF = no bias
STEP and DIR Outputs:	Differential RS-422 drivers (No internal terminations)
User RS-422 Outputs	Differential RS-422 drivers (No internal terminations)

6.4 ENVIRONMENTAL

OPERATING TEMPERATURE:	0°C (min) to 50°C (max)
TEMPERATURE CHANGE	10°C per hour (max)
HUMIDITY	0% to 95% Relative Humidity, non-condensing
VIBRATION	1.5mm (0.060") P-P sinusoidal
SHOCK	30g half sine shock 11msec individual axis

Exceptions to the product vibration and shock are Ethernet connectors. The specifications for the Molex 85504-0001 modular jacks used on the production RMB modules are as follows:

MFGR Spec:	Molex PS-85505 FCC Part 68, Subpart F
Vibration:	1.5mm (0.060") P-P 10-55-10 Hz sweep per minute 2 hours in each X-Y-Z axis No discontinuities greater than 1 usec
Shock:	50g three sawtooth waveform shocks in each X-Y-Z axis No discontinuities greater than 1 usec
Mating Family:	95043 Series

Note that the RMB product family provides for the use of cable support brackets with Ethernet cables plugged into connectors J1 and J2. See the Appendix A for additional details.

6.5 COOLING REQUIREMENTS – TA801

The TA801 RMB can dissipate 7.7W internally. Convective cooling requires mounting the RMB vertically, as shown below. 1.5 inches of clearance is required both above and below the module for convective cooling airflow.

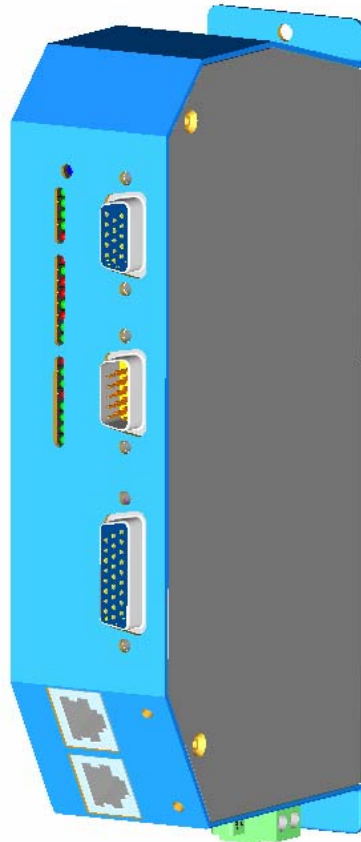


FIGURE 26 – TA801 MOUNTING VIEW

For special mounting considerations or environments, internally mounted fan-forced cooling is available as a manufacturing option. For available product options see Appendix A. When the internal forced cooling is used the RMB module may be mounted either horizontally or vertically. It should not be mounted in an inverted orientation (meaning with J3 on top).

6.6 COOLING REQUIREMENTS – TA802

The TA802 RMB can dissipate up to 8.9W internally. Convective cooling requires mounting the RMB vertically, as shown below. 1.5 inches of clearance is required both above and below the module for convective cooling airflow.

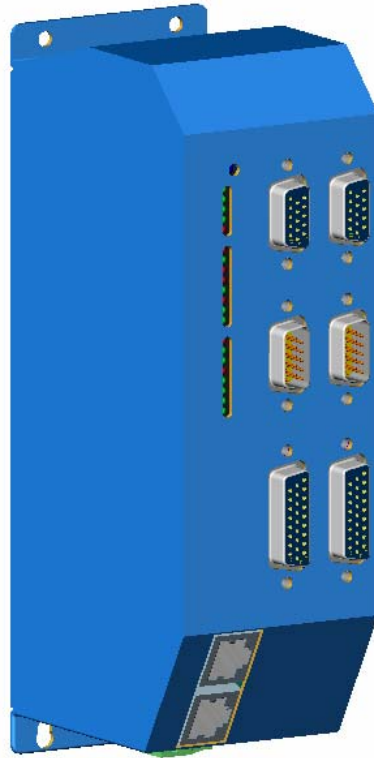


FIGURE 27 – TA802 MOUNTING VIEW

For special mounting considerations or environments, internally mounted fan-forced cooling is available as a manufacturing option. For available product options see Appendix A. When the internal forced cooling is used the RMB module may be mounted either horizontally or vertically. It should not be mounted in an inverted orientation (meaning with J3 on top).

7 SOFTWARE

This section discusses required software and firmware levels for the RMB and host system. There is also a brief explanation of how node alarm is generated for the TA801 and TA802 RMB module family.

7.1 REQUIRED SOFTWARE LEVELS

The RMB requires certain minimum revision levels of software and firmware in order to function correctly. These required minimum levels are:

MPI Firmware:	Version 510 Option 0
MPI DLL:	Version 20031023
MPI Version:	Version 20031023
MEI Host Firmware:	XMP510A1
FPGA Runtime Version:	0x020E0300

Please note that TA801 and TA802 RMB Modules are shipped without a FPGA Runtime image loaded. This provides the customer with the opportunity to assure that the Runtime image correct for his current network level can be loaded into the module after installation.

7.2 NODE_ALARM GENERATION

Both the TA801 and TA802 RMB modules have a status LED (D6) on the front panel that indicates alarm status. This LED is illuminated when a NODE_ALARM state exists. The node can generate this alarm based on numerous inputs.

NODE_ALARM is always active during power-on-reset, and during FPGA hardware configuration. This is due to external termination on the FPGA. NODE_ALARM is also active while the FPGA BOOT image is being loaded from Flash. Once the FPGA is configured with the RUNTIME image, software can configure the FPGA NODE_ALARM and I/O_ABORT mask registers. The FPGA defaults to having NODE_ALARM active when the network is not up. Software can override this during the discovery process. An active I/O_ABORT state or a NODE_ALARM state will create an alarm only if the mask registers have been configured to allow the fault to propagate.

The inputs to the mask register for the FPGA NODE_ALARM signal are:

- I/O_ABORT
- Node Not Cyclic
- AMP_FAULT Axis 0
- AMP_FAULT Axis 1

These fault sources can be individually masked or enabled by software. Note that in the TA801 and TA802 RMB designs, the AMP_FAULT inputs from each axis consist of the following sources:

- AMP Fault (from FAULT input on J5 pin 3)
- RT Fault (thermal shutdown signal for BRAKE and USER OUT drivers)
- MT Fault (thermal fault from module internal temperature sensor)

- Feedback Fault (from FPGA encoder module, can be illegal state or broken wire detected)

The inputs to the mask register for the I/O_ABORT signal are:

- Sync Lost (the node has lost the SYNQ signal, and therefore is no longer under software control)
- Node disable (from SHUTDOWN inputs on J6-0 or J6-1)
- Analog Power Fault (+15V and -15V monitor internal to module)
- User (trigger from controller memory address)

These fault sources can be individually masked or enabled by software.

Note that an I/O Abort state will force the DAC outputs to 0Vdc, and will force all FPGA I/O pins to be inputs, thus tri-stating all outputs. Termination external to the FPGA will keep all I/O circuitry in required default states.

7.3 DAC CONTROL

The DAC's used on the TA801 and TA802 RMB modules are configured for 16-bit, bipolar operation. The DAC's output's will reset to 0.0Vdc, and are non-glitching during power-on reset and configuration. Example DAC settings are as follows:

DAC Count	Output Voltage (Vdc)
0x7FFF	+9.997
0x4000	+4.997
0x1000	+1.248
0x0000	0.000
0xF000	-1.251
0xC000	-5.002
0x8000	-10.003

Table 11 – DAC Output Values

APPENDIX A – PRODUCT OPTIONS

TA801 and TA802 products can be ordered with several options. These options are detailed in the following section.

Ethernet Cable Clamp Option

A cable clamping option may be attached to any TA801 or TA802 RMB module. When attached, this bracket clamps the Ethernet cables in place, minimizing movement of the Ethernet cables relative to the module. The cable clamping option is ordered as:

P/N: SUBZ-0803-A01

Cooling Fan Option

Any TA801 or TA802 RMB module may be ordered with a cooling fan option. This 2.0 CFM fan, installed internally to the module during manufacturing, is recommended if horizontal mounting is expected. The fan option is ordered as shown in the following table:

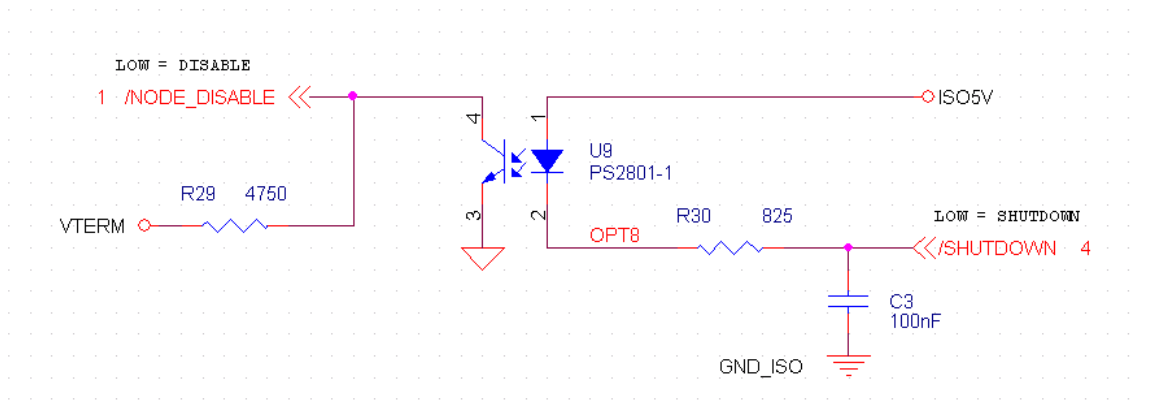
Product Family	P/N without Fan	P/N with Fan
TA801	TA801-D01	TA801-D21
	TA801-E01	TA801-E21
	TA801-F01	TA801-F21
TA802	TA802-D01	TA802-D21
	TA802-E01	TA802-E21
	TA802-F01	TA802-F21

Table 12 – Fan Option Numbering

APPENDIX B – HARDWARE ERRATA

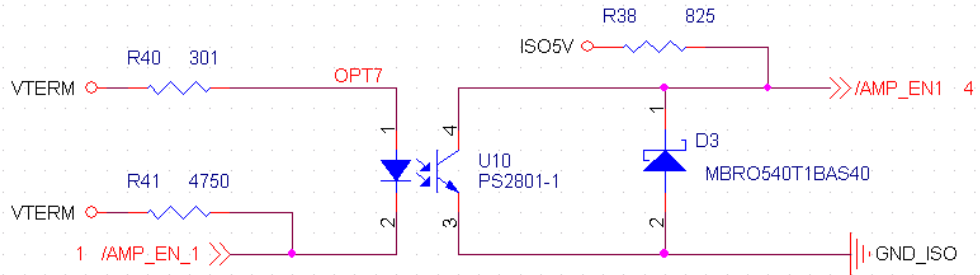
Hardware changes occurred during the development of the TA801 and TA802 RMB products. These changes are detailed below.

- Early prototype TA801 and TA802 RMB modules (containing SMC PCB-0800-01 Rev 1) were shipped to beta-sites with Ethernet connectors that would not guarantee isolation between the connector shields and the chassis. This was revised after the first round of prototypes.
- Prototype RMB modules used AMP 406541-1 (or -5) for the Ethernet connectors. After the first prototype run the connectors were changed to Molex 85504-0001.
- Prototype TA801 and TA802 RMB modules had single-ended SHUTDOWN input circuits on axis 0. The axis 0 (MC1) input circuit was an active-low 5V OPTO input. Connecting the input pin to ground or a logic low signal would assert SHUTDOWN and create a node alarm.



- RS-422 transceiver outputs for STEP and DIRECTION were swapped between axis 0 and axis 1 on early prototype RMB TA801 and TA802 modules. These were corrected as of the pilot build.

- Prototype and early revision RMB modules used a single-ended output model for the axis 1 (MC2) Amplifier Enable output circuit. The axis 1 (MC2) output circuit was an emitter-grounded active-low 5Vdc OPTO output stage.



APPENDIX C – CONTACT INFORMATION

Do you have hardware Questions?

Any hardware questions regarding use and operation of the Trust Automation TA801 and TA802 RMB family of products should be directed to:

Trust Automation, Incorporated
205 Suburban Road
San Luis Obispo, CA 93401

Corporate Office Telephone: (805) 544-0761
Corporate Office Facsimile: (805) 544-4621

Corporate Website: www.trustautomation.com
Email: support@trustautomation.com

Do you have software Questions?

Any questions regarding use and operation of MEI XMP software with the TA801 and TA802 RMB family of products should be directed to:

Motion Engineering, Incorporated
33 South La Patera Lane
Santa Barbara, CA 93117-3214

Corporate Office Telephone: (805) 681-3300
Corporate Office Facsimile: (805) 681-3311

Corporate Website: www.motioneng.com and www.support.motioneng.com
Email: info@motioneng.com

Additional information regarding the SynqNet Interface Standard can be found at:

http://www.synqnet.org/tech_library.html

Additional information regarding connectors and other components can be found at the following websites:

Molex Website: http://www.molex.com/cgi-bin/bv/molex/index_login.jsp

Phoenix Contact Website: <http://www.phoenixcon.com/>

Tyco/Raychem Website: <http://www.raychem.com/>

Kycon Website: <http://www.kycon.com>

NORCOMP Website: <http://www.norcomp.net/>

APPENDIX D – WARRANTY STATEMENT

Trust Automation Inc. (Limited 1 Year Warranty)

GENERAL - All hardware products sold by Trust Automation Inc. are warranted against defects in material and workmanship for a period of **one (1) year** from the date of shipment. If you believe a Trust Automation Inc. hardware product you have purchased has a defect in material or workmanship, or has failed during normal use within the warranty period, please contact Trust Automation Inc. at (805) 544-0761 for assistance and/or a Return Material Authorization Number (RMA#).

If product repair or replacement is necessary, the Customer will be responsible for all return shipping charges, freight, insurance and proper packaging to prevent damage in transit, whether or not the product is covered by this warranty. During the warranty period, product determined by Trust Automation Inc. to be defective in form or function will be repaired or, at Trust Automation Inc.'s option, replaced at no charge. Trust Automation Inc. will pay the return shipping charges (ground for US based shipments, most economical air for international shipment. Customer may elect to change shipment method and pay the difference.), for products that have been repaired or replaced. All duties and taxes remain the responsibility of the customer. All shipments of repaired or replaced products will be F.O.B. at Trust Automation Inc. headquarters in San Luis Obispo, California.

For tracking purposes, products to be repaired or replaced must be returned to Trust Automation Inc. with a Trust Automation Inc. RMA#, and a Purchase Order. The standard charge for non-warranty repair work is \$120 per hour, plus parts. Trust Automation will provide repair cost estimate prior to performance of out of warranty repair work.

Material and workmanship used in the repair and replacement of Trust Automation products under this warranty are warranted additionally against defects for a period of ninety (90) days from the date of return shipment to the customer.

LIMITATIONS - This warranty does not apply to damage resulting from accidents or any Customer actions, such as mishandling, misuse, improper interfacing, operation outside of design limits, improper repair, or unauthorized modification. No other warranties are expressed or implied. Trust Automation Inc. liability shall be limited to the actual purchase price of any defective unit or units of equipment to which a claim is made, and shall in no event include the Customer's manufacturing costs, lost profits or goodwill, or any other direct, indirect, special, incidental or consequential damages.

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